

ECE 445

Spring 2025

Project #3: CCD Image Sensor Board for Film Camera Retrofit

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1. Introduction

1.1 Problem

The sudden explosion of demand for old CCD sensor equipped cameras amidst the digicam trend [1][2] is mismatched against a supply of 10-20 year old cameras that are increasingly unreliable and outdated. Between strong consumer demand for these out-of-production cameras, a rise in age-induced failures, and a shortage of outdated, scarce accessories such as proprietary batteries and obsolete storage cards, functioning examples of these CCD cameras are now very difficult to obtain and more fragile than ever.

1.2 Solution

Our project is creating a new source of reliable CCD sensor cameras. We will create a PCB that accepts commonly available salvaged CCD sensors and drops them into an advanced film camera. We can minimize our PCB's BOM cost and maximize reliability and compatibility by pairing these salvaged CCD sensors with modern microcontrollers and components, and the plentiful supply of advanced film cameras will ensure that this conversion is practical. The rising price of film [3] has created a glut of technologically advanced film cameras that are cheap to purchase in working condition but too expensive to operate (akin to an inkjet printer).

In practice, our PCB and resulting conversion will emulate the Kodak DCS460 from 1995, but much smaller and modernized to 2025. The PCB will contain the Sony ICX-453 CCD sensor, accompanying power supply, driving, and A->D conversion circuitry, an STM32 microcontroller with SDRAM buffer, an SD card slot, Li-Ion BMS for replaceable 2S 18650 cylinder cells, and buttons and 7-segment displays for user interface. The PCB will be installed into a 3D printed enclosure ("Module") that also holds the batteries and interfaces with the Nikon N90s camera ("Host Camera"), and the Module will synchronize with the Host Camera through its Nikon 10-pin serial interface.

1.3 Visual Aid



Fig. 1: High level implementation of solution depicting old camera to be harvested and the final product that our solution would resemble. Please note that our solution would be a lot more compact than the depicted model

1.4 High-level requirements list

- The completed module will connect to the Nikon N90s camera, and it will save 6 Megapixel color images in uncompressed RAW format.
- The UI will consist of, at minimum, 3 buttons (Delete, Navigate, Select) and a dot-matrix display for status readout.
- The module will accept and save images to SDHC/SDXC cards of at least 32GB capacity.
- The module can be charged over USB-C.
- The N90s camera and module will shoot at a rate of 1 picture per second, with no loss of data.

2. Design

2.1 Block Diagram

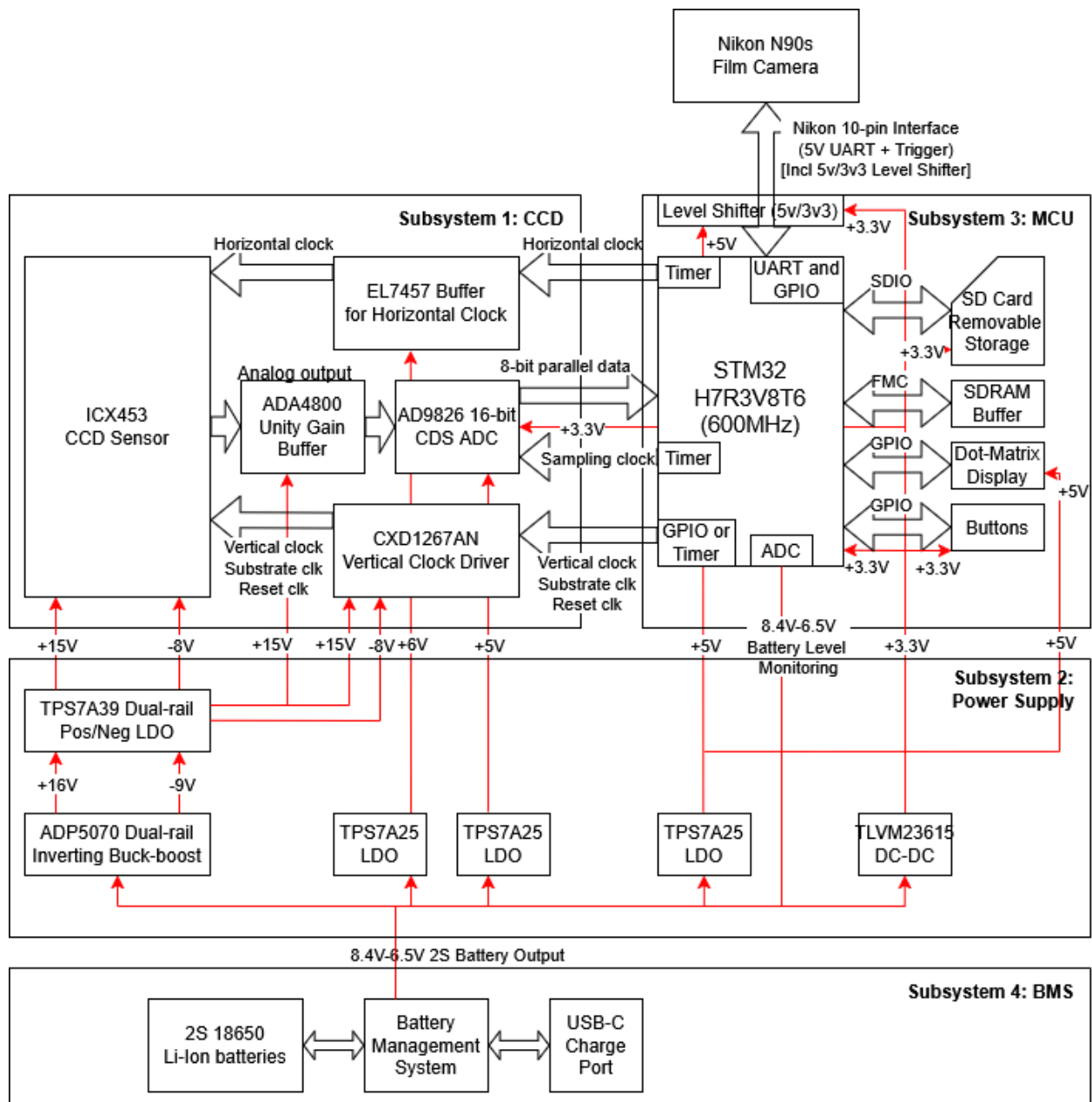
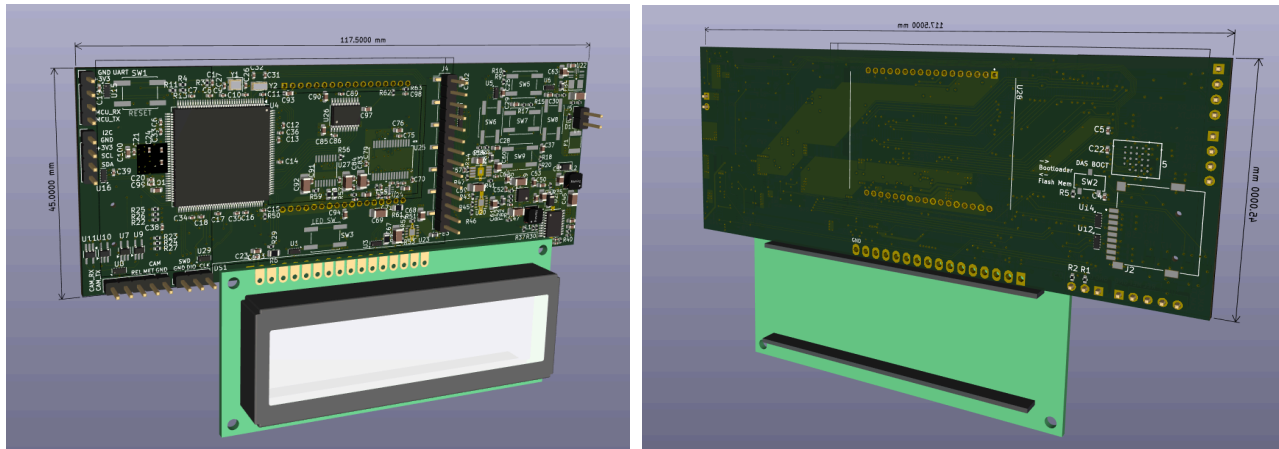


Fig 2. Block diagram representing subsystems connected throughout the PCB and module.

2.2 Physical Design

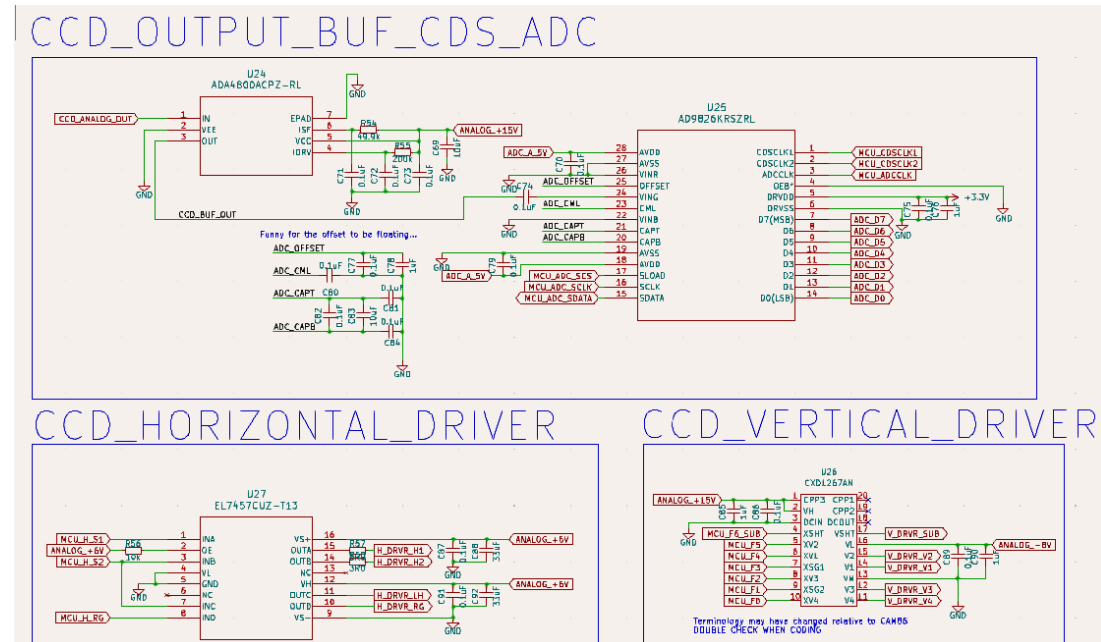


Precise measurements were noted for the camera's dimensions and the PCB was designed so as to fit in place of the back door. Special care was taken to place components where they would not interfere with the camera as is evident by the rather barren backside of the PCB. The tight dimensional constraints and the inability to use the backlayer forced us to rely on a 4-layer PCB instead of a 2-layer one to keep the signal level noises down to a minimum. Furthermore, as can be seen in the PCB, several breakout points were incorporated into the design to allow us to be able to add additional functionality given the time.

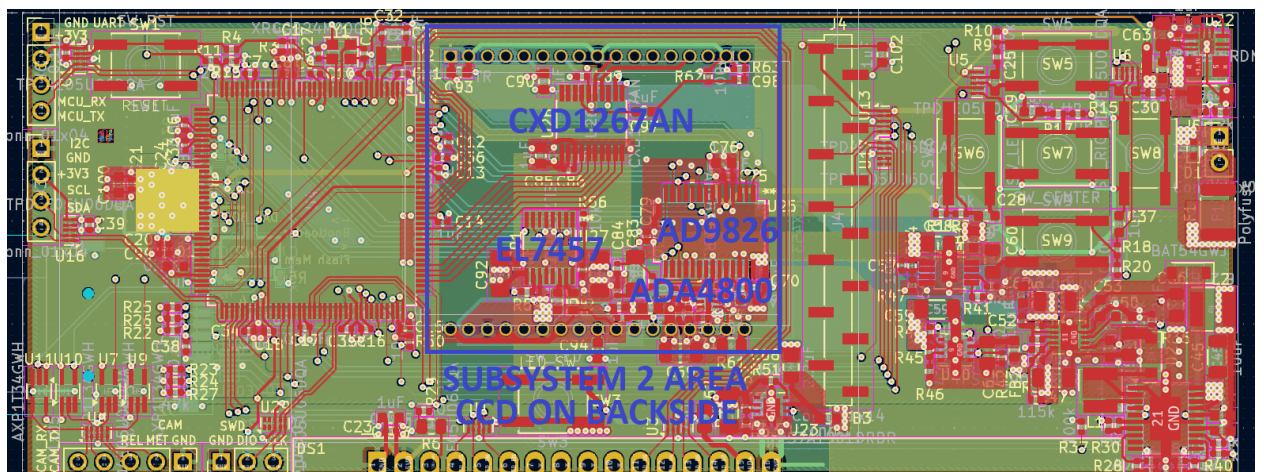
2.3 Subsystem Overview

2.3.1 Subsystem 1: CCD sensor, driving circuitry, and A-D

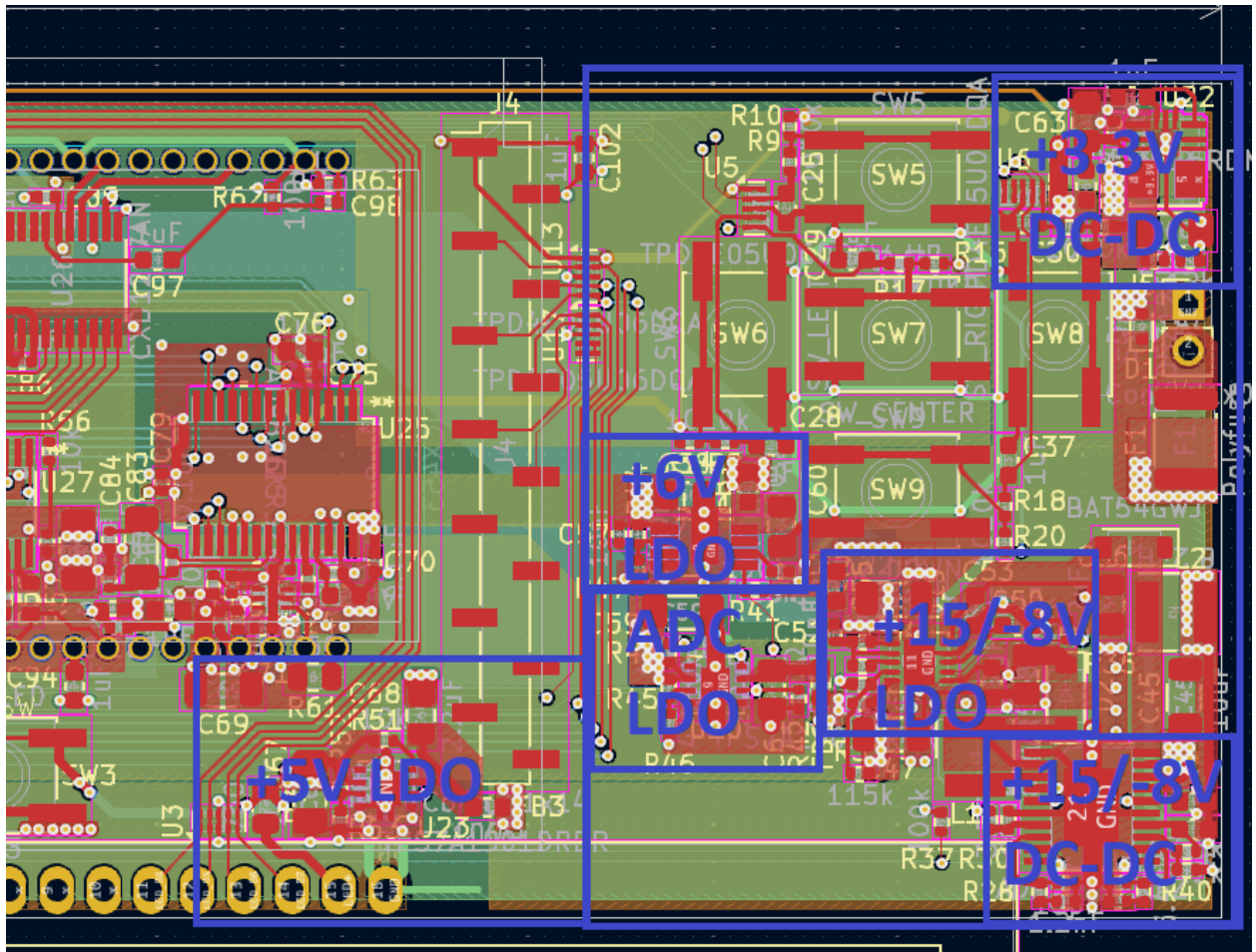
Subsystem 1 is responsible for properly driving the CCD sensor, and it sends digitized pixel data to Subsystem 3. We are intimately aware that driving the CCD sensor is not only the most critical and irreplaceable part of our project but also the most error-prone part of our project. Thus, our design borrows many aspects of the parts selection, operation, and schematic of Subsystem 1 from the well-proven open-source CAM86 [4][5][6][7][8] astrophotography camera project.



This subsystem includes the Sony ICX-453 CCD sensor as salvaged from old cameras, CXD1267 CCD vertical clock driver, EL7457 horizontal clock driver, ADA4800 low-noise buffer, and AD9826 16-bit CDS ADC. We have put additional emphasis on verifying this design and ensuring that it can stand up to the higher frequency of our new 600MHz MCU and 12.5MHz target CCD clock rate (in contrast to the 8MHz MCU and variable ~4MHz CCD clock rate of the original design).



2.3.2 Subsystem 2: Power supply system



The ICX453 CCD sensor requires +15V, -8V, and +6V and may draw moderate current at times due to its large capacitances. Additionally, the supporting circuitry in Subsystem 1 and Subsystem 3 (Microcontroller, SDCard, and UI) will require 5V and 3.3V rails to support their components. This totals to 5 discrete voltages used in our project, powered by 2s Lithium Ion battery cells (a source that varies between 6.5-8.4V)

The power supply architecture for our project primarily targets low noise and secondarily targets a small footprint and good power efficiency. Low noise is necessary since Subsystem 1 is partially analog and generates digital picture data, so best picture quality requires careful power rail noise suppression. Footprint and power efficiency considerations are driven by the desire to minimize Size, Weight, and Power (SWAP) on a hand-held, battery-powered device.

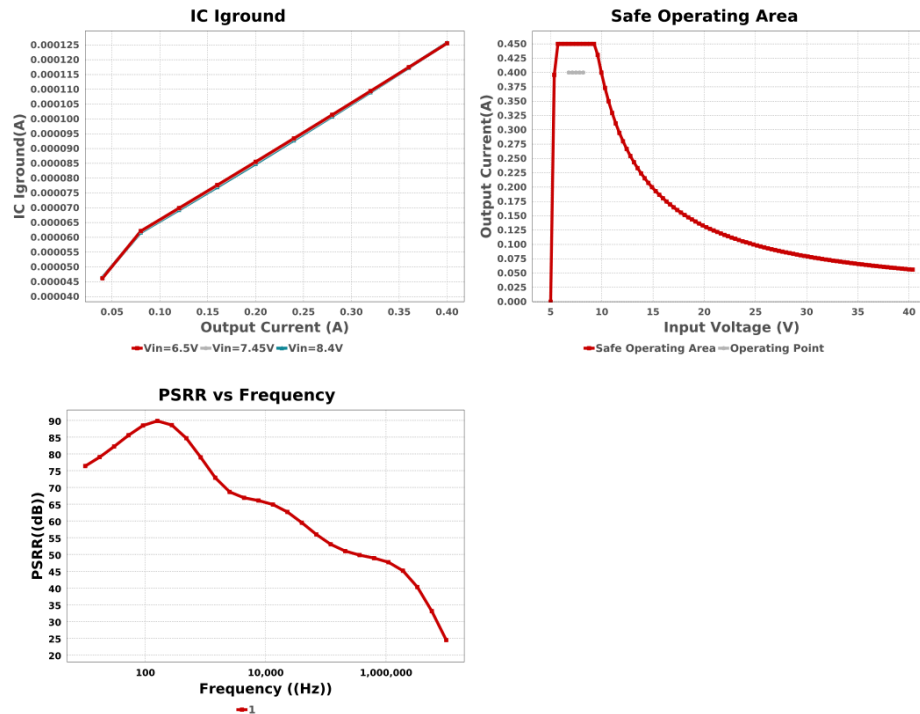
Correspondingly, we are implementing a multi-rail power supply architecture that emphasizes compactness and low noise.

- +15V and -8V used by Subsystem 1 are created by DC-DC boost conversion (ADP5070) followed by low-noise LDO regulators (TPS7A39). Boost conversion is necessary to generate the negative voltage and the greater positive voltage

with sufficient efficiency, while the LDO removes noise and isolates load transients.

- +6V used by Subsystem 1 is created by an LDO (TPS7A1901). This model is selected for relatively high current and good transient characteristics, as well as low noise and component count compared to buck converter solutions. The small drop from battery voltage also means that an LDO does not sacrifice much efficiency compared to a switching converter. The +6V rail especially emphasizes transient performance, since the CCD horizontal clock switches a load very frequently.

The below graphs demonstrate why this LDO was selected: high PSRR at the expected noise frequency (1MHz of DC switching supply and 12MHz of CCD clock), low quiescent current, and safe high-current operation at the expected input battery voltage levels. Values calculated using TI WEBENCH POWER.



- +5V used by Subsystem 3 is created by another LDO (TPS7A1901 again) primarily due to simplicity. While a switching converter would be more efficient, this is a lightly loaded rail primarily used for signalling.
- +5V used by the ADC in Subsystem 1 has a dedicated rail served by a special low-noise LDO (TPS7A49) in order to ensure the CCD readout analog circuitry is undisturbed by other component. We considered the efficiency loss compared to a switching component to be a worthy sacrifice.

The following specifications are highlighted to show our selection criteria. Values calculated using TI WEBENCH POWER.

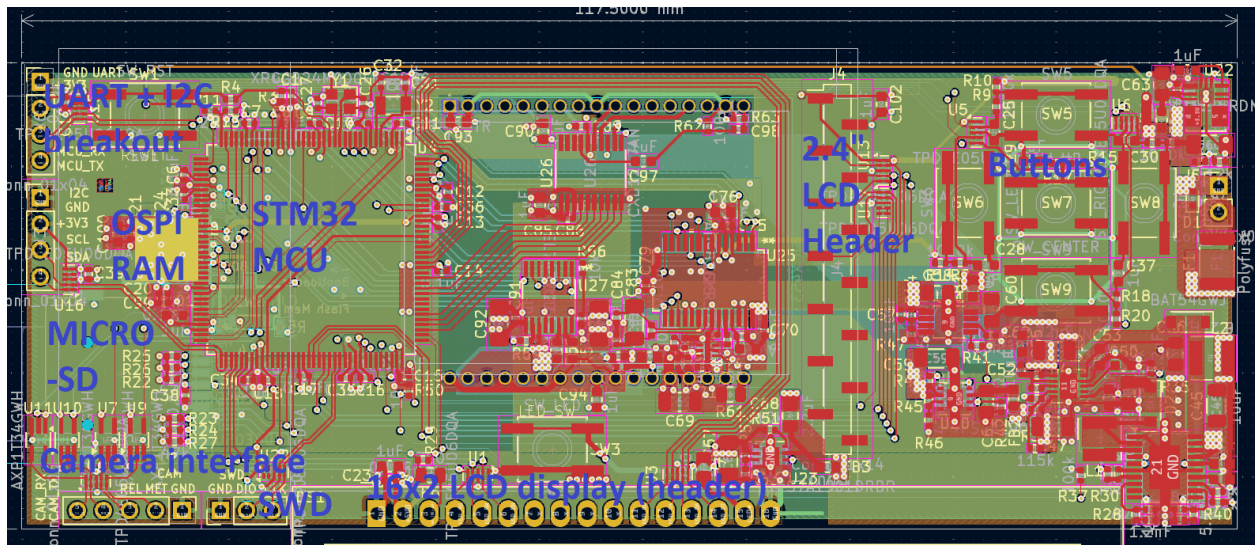
Operating Values

#	Name	Value	Category	Description
1.	Output Noise RMS	22.134 μ V	General	Noise RMS
2.	IC Iground	853.814 μ A	IC	IC ground current
3.	IC Pd	347.172 mW	IC	IC power dissipation
4.	IC Tj	52.011 degC	IC	IC junction temperature
5.	IC Tolerance	29.7 mV	IC	IC Feedback Tolerance
6.	ICThetaJA	63.4 degC/W	IC	IC junction-to-ambient thermal resistance
7.	Iin Avg	100.85 mA	IC	Average input current
8.	IOUT_OP	100.0 mA	Op Point	Iout operating point
9.	Input Ripple Frequency	10.0 MHz	Op Point	Input Source Ripple Frequency for PSRR Calculation
10.	PSRR est.	-47.72 dB	Op Point	Power Supply Rejection Ratio estimated
11.	VIN_OP	8.4 V	Op Point	Vin operating point
12.	Total Pd	347.172 mW	Power	Total Power Dissipation
13.	BOM Count	7	System Information	Total Design BOM count
14.	Efficiency	58.96 %	System	Steady state efficiency

- +3.3V used by Subsystem 3 uses an integrated-inductor switching DC-DC converter (TLVM23615) since the +3.3V rail is heavily loaded by relatively noise indifferent digital devices. Integrated inductor solutions are small, cheap, and reduce part count.

Layout focused on isolating noise sources and maximizing current handling capacity. All of layer 3 was dedicated to power routing, and some of the back layer when rails overlapped. Vias were used extensively to ensure power planes and devices were well connected, rails with high transient loads received generous bulk capacitance (still within regulator specification), and special care was taken to ensure that all passives were well within operating tolerances even with temperature or age derating. Low ESR tantalum capacitors with generous voltage rating margin were used when X7R ceramics could not supply sufficient capacitance at the expected DC bias.

2.3.3 Subsystem 3: MCU, camera I/O, SDCard, User Interface



Subsystem 3 consists of an STM32H7R3Z8T6 MCU, 128Mbit OSPI PSRAM buffer, SWD programming port, microSD card slot, user-accessible buttons, 16x2 LCD display, and 2.4" color 320x240 LCD display. The MCU will be responsible for the following:

- Controlling Subsystem 1 and receiving its image data. Clocks are generated with onboard timers or GPIO pins, and image data will be received with the DCMIPP/PSSI interface or GPIO pins.
- Controlling Subsystem 2 to implement power saving functionality. This is accomplished with GPIO pins.
- Monitoring battery voltage from Subsystem 4. This is accomplished with the onboard ADC.
- Synchronizing with the Host Camera through the camera's Nikon 10-pin interface (including a triggering signal and a serial interface for querying the camera's state and configuration)
- Buffering images to OSPI PSRAM to enable rapid shooting
- Processing and saving images to the microSD over SDIO, maximizing readout speed to flush the buffer as quickly and possible
- Accepting user inputs via button press and reacting accordingly, including configuration changes and a delete button that erases the most recently saved file. This will include the user-accessible power button, so that a power-off does not cause data loss.
- Driving the 16x2 LCD for module state and status readout
- Driving the color 2.4" LCD display to display captured images or other graphics

We originally specified the STM32H7R3V8T6 (100 pin LQFP package), but at this point we are committed to using the 144 pin variant STM32H7R3Z8T6 instead. This is due to the insufficient pinout on the original part, as we have now added provisions for additional components such as a GPS module for geotagging and a light sensor for color balance. The STM32H7 family was retained due to its high clockspeed, high-speed I/O, significant processing power, SDIO capability, XSPI PSRAM interface, and JPEG engine for real-time JPEG compression at minimum cost. JPEG compression and requisite Bayer conversion, image playback, GPS tagging, or light sensing are still not part of the success criteria, but allocating for these features at this time is a worthwhile investment as they would significantly enhance the camera's practical usability.

This excerpt from the datasheet is highlighted to show the specific features of the STM32H7 that convinced us to use the platform:



STM32H7R3x8 STM32H7R7x8

Arm[®] Cortex[®]-M7 32-bit 600 MHz MCU, 64 KB flash, 620 KB RAM, Ethernet, 2x USB, 2x FD-CAN, advanced graphics, 2x12-bit ADCs

Datasheet - production data

Features

Includes ST state-of-the-art patented technology

Core

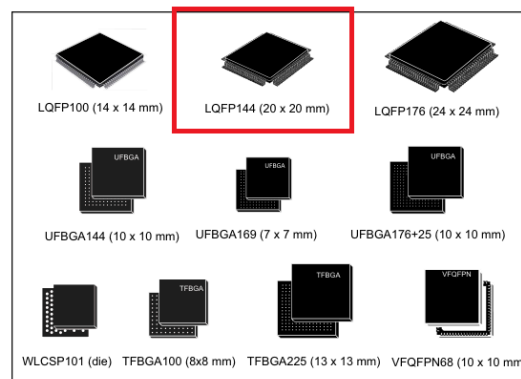
- 32-bit Arm[®] Cortex[®]-M7 CPU with MPU and DP-FPU, L1 cache: 32+32-Kbyte instruction and data cache allowing 0-wait state execution from embedded flash memory and external memories, frequency up to 600 MHz, 1284 DMIPS/2.14 DMIPS/MHz (Dhrystone 2.1), and DSP instructions

Memories

- Up to 2x octo-SPI memory interfaces or 1 octo-SPI + 1 hexa-SPI with XiP, with support for serial PSRAM/NAND/NOR, HyperRAM™/HyperFlash™ frame formats running at up to 200 MHz

2x DMA controllers to offload the CPU

- 2 × dual-port DMAs with FIFO and linked listed support



Graphics

- Hardware JPEG codec

23 timers

- Sixteen 16-bit (including 5 x low power 16-bit timer available in stop mode, one graphic timer), four 32-bit timers, 2x watchdogs, 1x SysTick timer

Up to 35 communication interfaces

- 3 × I2C FM+ (SMBus/PMBus™)
- Up to 3 USARTs/4 UARTs (ISO7816 interface, LIN, IrDA, modem control) and 2x LPUART
- 6 SPIs with 4 with muxed duplex I2S and 3x USART configured in synchronous mode
- 16-bit parallel slave synchronous interface

As Subsystem 1 is largely based on the CAM86 [4][5][6][7][8] project, some of the code from CAM86 [4][5][6][7][8] may also be referenced or borrowed to form the interface between Subsystem 3 and Subsystem 1. Any borrowed code will require substantial revision due to the integration of substantially more functionality in this project, and the use of an STM32 MCU as opposed to CAM86's [4][5][6][7][8] AVR MCU.

Subsystem 1 layout prioritized signal integrity, with high-speed devices such as the OSPI PSRAM, SDcard, and communication with the ADC and clock drivers being routed first. Slow clocks and toggled signals were routed afterwards, on rather convoluted paths. Trace lengths were painstakingly matched to be within SDcard and PSRAM tolerances, and trace widths were selected in accordance with impedance calculations according to spec sheets. The entirety of the second layer of the PCB was a ground plane, and should serve to shield signals quite effectively from interference; further

shielding ground traces and dedicated ground return paths were added to minimize the possibility of noise issues. All devices received high-frequency decoupling capacitors on all power pins without exception.

2.3.4 Subsystem 4: Battery Management System

Subsystem 4 consists of an integrated BMS system (BQ25886) and a USB-C charging port for the 2S 18650 Li-Ion power source, as well as a power kill switch for use during debug and assembly. This subsystem integrates primarily with Subsystem 2 (Power regulation), and Subsystem 3 (MCU) to enable a user-visible battery level readout.

The BMS provides short circuit and overcurrent protection, as well as overcharge and over-discharge protections to the sensitive and dangerous Li-Ion battery cells. The BMS system charges the battery cells from a USB-C port that is exclusively used for charging. We may incorporate USB-C fast-charging capability, but it will not be part of this project's success criteria.

The following datasheet capture highlights the choice of BQ25886 for our purposes.

BQ25886 Standalone 2-Cell, 2-A Boost-Mode Battery Charger With PowerPath, USB BC1.2 Detection, and USB On-The-Go Boost (OTG)

1 Features

- High-efficiency 2-A, 1.5-MHz switch mode boost charger
 - 93.4% Charge efficiency at 5-V adapter, 7.6-V battery, 1-A charge
 - Optimized for USB input and 2-cell Li-Ion battery
- Single input to support USB input adapters
 - Supports 4.3-V to 6.2-V input voltage range with 20-V absolute maximum input voltage rating
 - Input current limit (500 mA to 3.3 A) to support USB2.0, USB3.0 standard adapters
 - Integrated USB D+/D- auto-detect USB SDP, CDP, DCP, and non-standard adapters
- Standalone function with PowerPath management
 - Highest battery discharge efficiency with 17-mΩ battery discharge MOSFET
 - Narrow VDC (NVDC) PowerPath management
 - Instant-on works with no battery or deeply discharged battery
 - Ideal diode operation in battery supplement mode
 - Adjustable charge voltage with VSET pin supports 8.2 V, 8.4 V, 8.7 V, and 8.8 V
 - Adjustable charge current with ICHGSET pin supports 100 to 2200 mA
 - Adjustable input current limit with ILIM pin
- Input current optimizer (ICO) to maximize input power without overloading adapters
- High integration includes all MOSFETs, current sensing and loop compensation
- High accuracy
 - $\pm 0.5\%$ Charge voltage regulation
 - $\pm 5\%$ Charge current regulation
 - $\pm 7.5\%$ Input current regulation
- Safety
 - Battery temperature sensing in charge
 - Thermal regulation and thermal shutdown

2 Applications

- Wireless speaker
- Smart Speaker
- EPOS Printer
- Portable POS
- IP network camera

3 Description

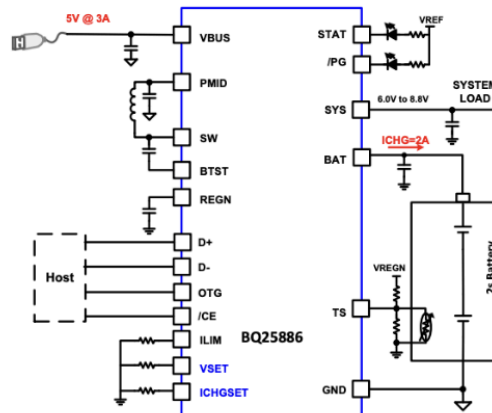
The BQ25886 is a highly-integrated 2-A boost switch-mode battery charge management and system PowerPath management which enables instant power on and provides accurate termination control device for 2-cell (2s) Li-Ion and Li-polymer battery. The BQ25886 is a standalone solution with PowerPath and OTG.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
BQ25886	VQFN (24)	4.00 mm x 4.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



2.4 Subsystem Requirements

2.4.1 Subsystem 1 Requirements:

- The CCD must return a usable 3000x2000 pixel image at a clock rate of 12.5MHz.
- The clock drivers, ADC, and other analog circuitry must function correctly at 12.5MHz.

2.4.2 Subsystem 2 Requirements:

- When taking an image, the +15V power rail for Subsystem 1 must operate continuously at +/-5% regulation, given a battery voltage of 8.4V or 7V.
- When taking an image, the -8V power rail for Subsystem 1 must operate continuously at +/-5% regulation, given a battery voltage of 8.4V or 7V.
- When taking an image, the +6V power rail for Subsystem 1 must operate continuously at +/-5% regulation, given a battery voltage of 8.4V or 7V.
- When taking an image, the +5V power rail for Subsystem 1 must operate continuously at +/-5% regulation, given a battery voltage of 8.4V or 7V.
- When taking an image, the +5V power rail for Subsystem 3 must operate continuously at +/-5% regulation, given a battery voltage of 8.4V or 7V.
- When taking an image, the +3.3V power rail for Subsystem 3 must operate continuously at +/-5% regulation, given a battery voltage of 8.4V or 7V.
- Rails equipped with MCU toggle control must turn on and off according to the MCU's instructions.

2.4.3 Subsystem 3 Requirements:

- The MCU must generate a 12.5MHz Horizontal clock for Subsystem 1.
- The MCU must be capable of buffering 12.5MB/sec image data from Subsystem 1.
- The MCU must sense the battery voltage to within 5%.
- The MCU must successfully save individual images to the SDcard without corruption or data loss, when images are taken at a rate of 1 image per second.
- The MCU must react to the Host Camera shutter.

2.4.4 Subsystem 4 Requirements:

- The BMS must cut off the battery output at or above 6.5V.
- The BMS must be able to charge the battery to above 8.0V and not above 8.6V.

2.5 Tolerance Analysis

The most critical component of this project is the CCD, as its absence or malfunction would negate the entire purpose of the project. It is not reasonable to simulate the complete functionality of the CCD, since it is a very complex analog device with minimal documentation that warrants too many unknown variables to simulate. However, we can use simulations to confirm that its supporting circuits are capable of supplying signals that meet the CCD's input specifications. The CCD has significant parasitic capacitances and requires certain rise and fall times on its clocks. We can accurately calculate if our driving circuitry is capable of meeting these timings and transient current requirements

using the equivalent circuit capacitances labelled on the CCD's datasheet and the known current carrying capabilities of the supporting circuits.

To test this, we constructed a simulation of the horizontal driving circuitry according to the CCD sensor's equivalent circuit. The EL7457 horizontal clock driver is specified to 2A current with an RDSon of 30 Ω , and the rise/fall times must be 5ns for 90% change. The LTSpice simulation below shows both these criterias are met; the transient current is around 1.2A and the rise/fall time for 90% change is around 3.3ns. With sufficient bulk capacitance, the +6V power supply should be capable of handling these momentary transients.

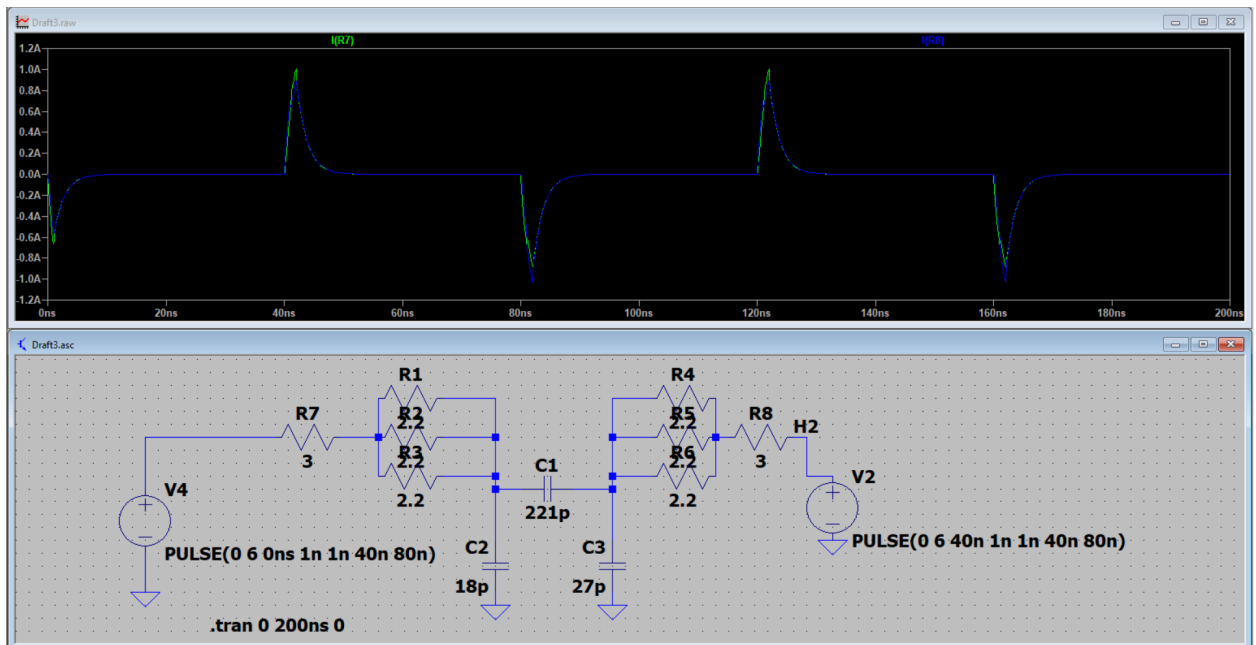


Fig. 3: LTSpice simulation depicting transient currents do not surpass the driver's specified limit.

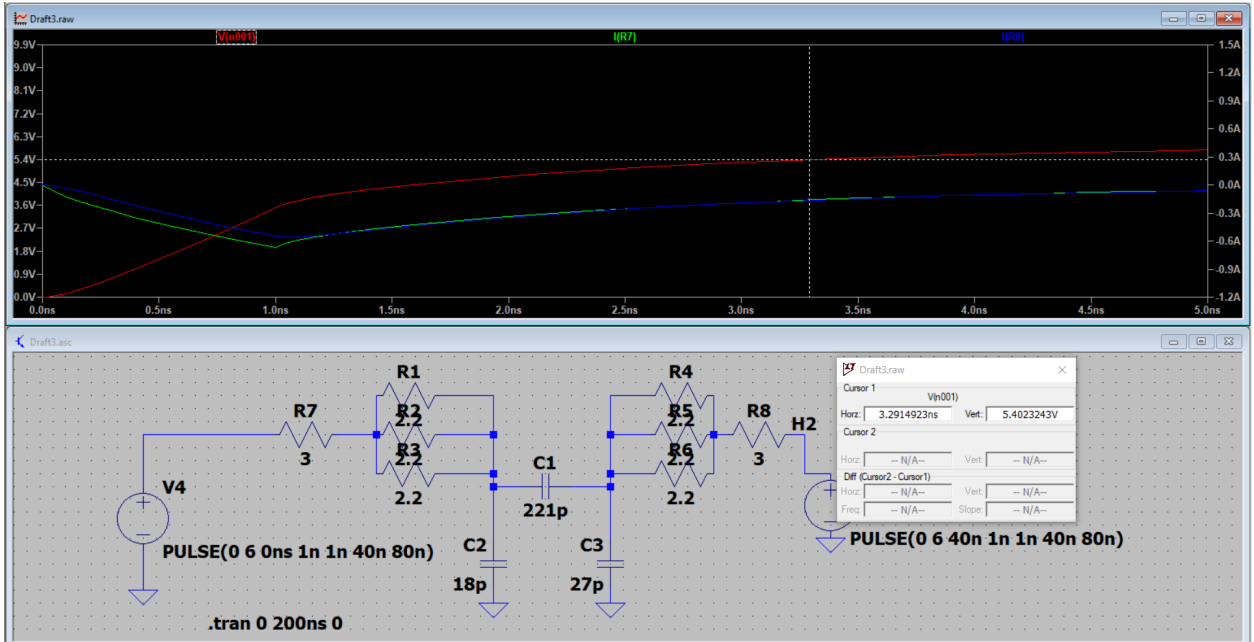


Fig. 4: LTSpice simulation depicting rise and fall times are within stipulated bounds.

is far beyond the proof of concept needed for this class. As such, we anticipate our labor costs as being unusually high.

$$\text{Labor cost estimate} = \$25/\text{hr} \times 2.5 \times 150 \text{ hours} = \$9,375$$

Total cost ~ \$9,500

3.2 Schedule

Week of	Plan of Action	Division of Labour
Mar 3, 2025	Finish ordering PCB and materials	All hands on deck
Mar 10, 2025	Solder PCB together and demo	All hands on deck
Mar 24, 2025	Finish the embedded systems work	All hands on deck
Mar 31, 2025	Reiterate if needed	All hands on deck

4. Ethics and Safety

4.1 Use of Open-Source Work

Our work builds upon a combination of open source projects ported to our specific needs, as such we recognize the ethical responsibility of properly attributing and adhering to licensing terms when reusing such work. In alignment with the ACM Code of Ethics (1.5), which promotes giving appropriate credit and respecting intellectual property rights, we will ensure that all borrowed concepts or code are properly cited and comply with the original licenses.

4.2 Reverse Engineering of Sensor Inputs

Due to the limited documentation available for CCD sensors, we may need to reverse-engineer some sensor inputs. We will ensure that this process does not violate proprietary rights or confidentiality agreements. The IEEE Code of Ethics (7.8.1.4) urges engineers to avoid engaging in practices that could be considered unlawful. As such, we will only use legally obtained resources and publicly available data for reverse engineering.

4.3 Battery Management and Power Safety

Since our device will utilize Li-ion batteries, we will integrate a Battery Management

System (BMS) to mitigate risks such as overcharging, overheating, or short-circuiting. This aligns with industry standards, such as IEEE 1725 for rechargeable battery safety. Furthermore, we will follow proper disposal and recycling guidelines as outlined in environmental regulations, ensuring compliance with both federal and state policies on battery waste management.

4.4 Laboratory Safety Compliance

Our development and testing will take place in University of Illinois laboratories, requiring strict adherence to campus safety policies. This includes compliance with electrical safety protocols, proper handling of PCB components, and adherence to lab-specific regulations to minimize hazards.

5. References

[1] JM. Farrell, "Digital cameras back in fashion after online revival," *BBC News*, Feb. 06, 2023. Available: <https://www.bbc.com/news/technology-64512059>

[2]G. Robles, "Why is Gen Z Obsessing Over Retro Digital Cameras?- 42West," *42 West, the Adorama Learning Center*, Feb. 23, 2023. <https://www.adorama.com/alc/retro-digital-cameras-gen-z/>

[3]B. Tridimas, "Why There's A Colour Film Shortage Right Now," *VICE*, Jan. 24, 2023. <https://www.vice.com/en/article/why-theres-a-colour-film-shortage-right-now/> (accessed Feb. 08, 2025).

[4] "Самодельная охлаждаемая ПЗС камера от grim - стр. 1 - Hand Made," *Kiev.ua*, 2025. <https://www.astroclub.kiev.ua/forum/index.php?topic=28929.0> (accessed Feb. 08, 2025).

[5]smr547, "GitHub - smr547/cam86: Build an CCD camera for astrophotography," *GitHub*, 2020. <https://github.com/smr547/cam86> (accessed Feb. 08, 2025).

[6]axsdenied, "GitHub - axsdenied/cam86_fw: Custom firmware for cam86 astro camera," *GitHub*, 2017. https://github.com/axsdenied/cam86_fw (accessed Feb. 08, 2025).

[7]vakulenko, "GitHub - vakulenko/CAM8_software," *GitHub*, 2025. https://github.com/vakulenko/CAM8_software/tree/master (accessed Feb. 08, 2025).

[8]“Cam86,” *Astroccd.org*, 2016. <http://astroccd.org/2016/10/cam86/> (accessed Feb. 08, 2025).