ECE 445

SENIOR DESIGN LABORATORY

Design Document

NeuroGuard

A Dual Electrocautery-Nerve Monitoring Device to Prevent Injury during Mastectomy

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Team No. 31

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1 Introduction

We provide details as to the problem we aim to address revolving around nerve injuries during masectomies, along with our proposed solution, in context.

1.1 Problem

Over 100,000 mastectomies are performed yearly in the U.S., with 40-60% resulting in nerve injury that can lead to a variety of symptoms, notably post-surgical pain [1]. In particular, damage to the intercostobrachial nerve (ICBN) is common during mastectomy and axillary lymph node dissection, a set of procedures common in treating metastatic breast cancer. Recently, surgeons have begun utilizing nerve-sparing techniques to ensure greater patient quality of life; however, these innovative techniques require meticulous dissection that can be complicated by anatomical variation and intraoperative bleeding.This highlights an urgent need for a device that provides real-time feedback to surgeons, enhancing safety and precision while also being easily integrated into existing workflows. To address this problem, we propose NeuroGuard, a device designed to alert surgeons when they are approaching the ICBN nerve during operations, thereby reducing nerve injury rates and improving patient outcomes.

1.2 Solution

Inspired by recent multifunctional surgical devices like a dual monopolar probe and suction tool, we are working with the NeuroGuard team to integrate contactless nerve detection and cautery functionalities into a single, cost-effective device. Over the course of the semester, we will work to design and simulate a circuit that demonstrates the ability to switch between predefined electrocautery and nerve stimulation waveforms at specified time intervals. We will

work to prototype this circuit that can be integrated with an electrosurgical unit and standard monopolar electrocautery probe. This project is a proof of concept for the hardware platform, demonstrating the capability to integrate power conversion and waveform generation that could be used with a standard cautery probe. The scope is strictly limited to the development and testing of this hardware; the detection of neural activation and the development of a feedback mechanism are considered future work beyond the scope of this project.

1.3 Visual Aid

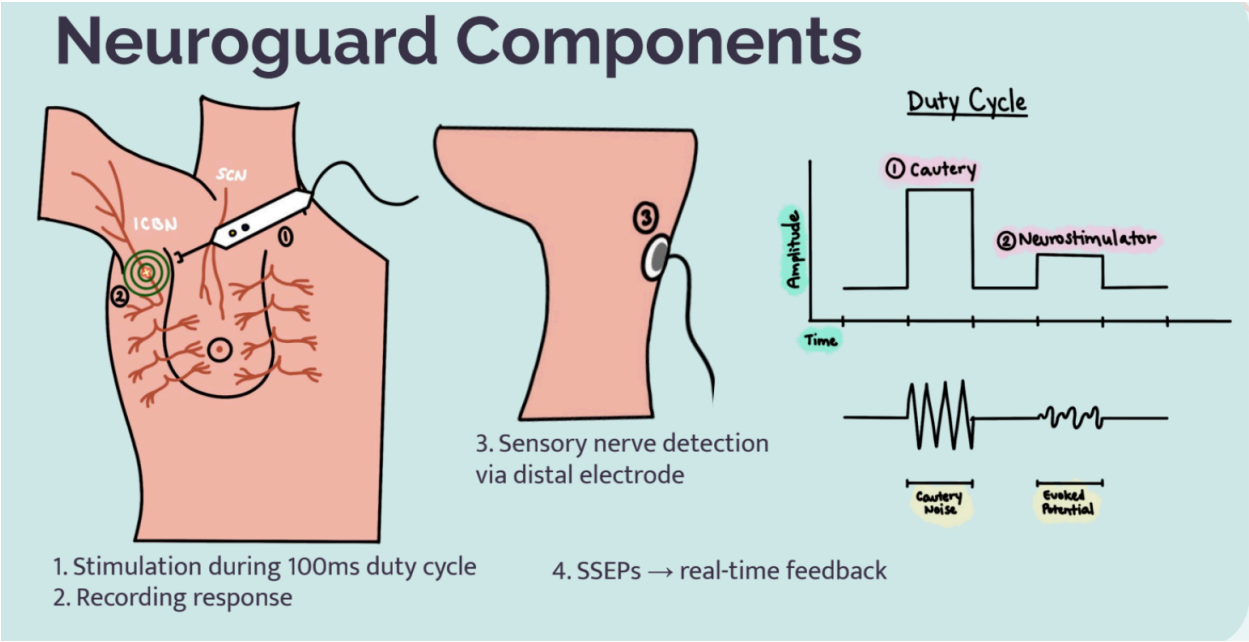

Figure 1: Overview of the Neuroguard system

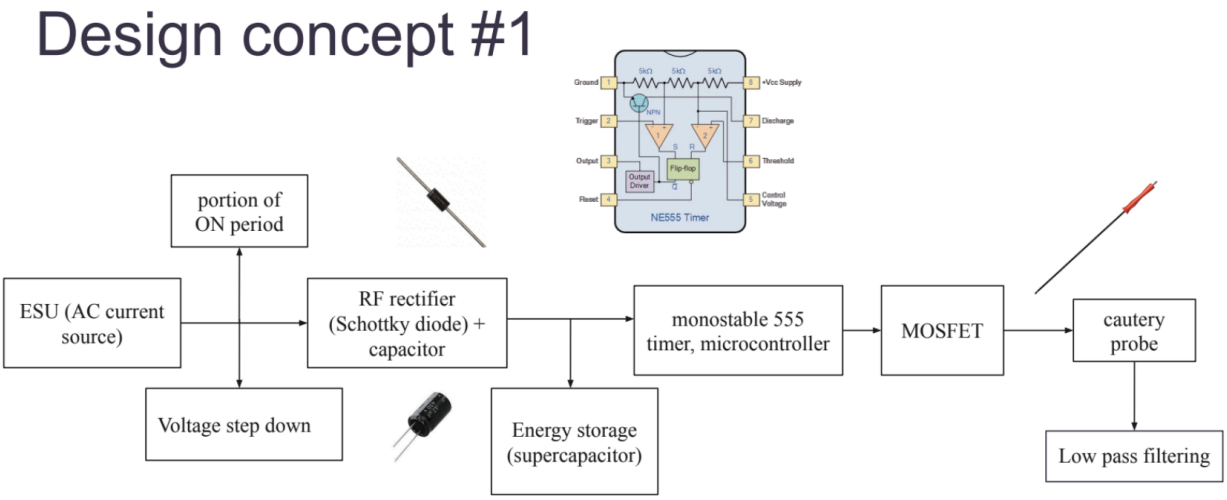

Figure 2: Initial design concept from the Neuroguard team

1.4 High-Level Requirements

To consider our project successful, we aim to accomplish the following goals:

1. Creation of 2000V to 5V step down converter system that is compatible with existing cautery power supplies
    a. Suitable sub systems for safe testing. This will involve a high voltage inverter and transformer to step down the voltage from 2000V to ~100V. This 100V AC will then go through a rectifier and buck converter to step it down to a suitable 5V that will be used by the circuit components.
2. Creation of suitable nervous stimulatory waveform from a 555 timer IC
3. Creation of a power MOSFET and a super capacitor to provide suitable pulsed current waveforms for neuron detection
4. Creation of interface hardware that will detect when to send out the nerve stimulating waveform.

1.5 Circuit Design

The system functions by employing pulse width modulation, alternating the standard cautery voltage settings with a smaller, pre-calculated neurostimulator waveform. These settings would reduce electrical noise interference, while enabling accurate downstream sensing of neural activation. The NeuroGuard system itself would reside between the electrosurgical unit (ESU) and the probe, modulating the waveform to include a component that allows for contactless activation of the ICBN. This modulation could occur by harvesting the existing power source of the ESU at specific time points within the duty cycle, or as an external power source that overlays the nerve-specific waveform onto the existing cautery duty cycle. In the first setup, the high-frequency AC current from the ESU would be rectified to a DC current, followed by a voltage step down mechanism and filtering. A supercapacitor can serve as the charge storage mechanism, with the discharge timed by a MOSFET, 555 timer, or other pre-programmed timing component. In the second setup, an external power unit, rather than the ESU, can be the source of the nerve-specific stimulation waveform.

2. Design Overview

2.1 Block Diagram

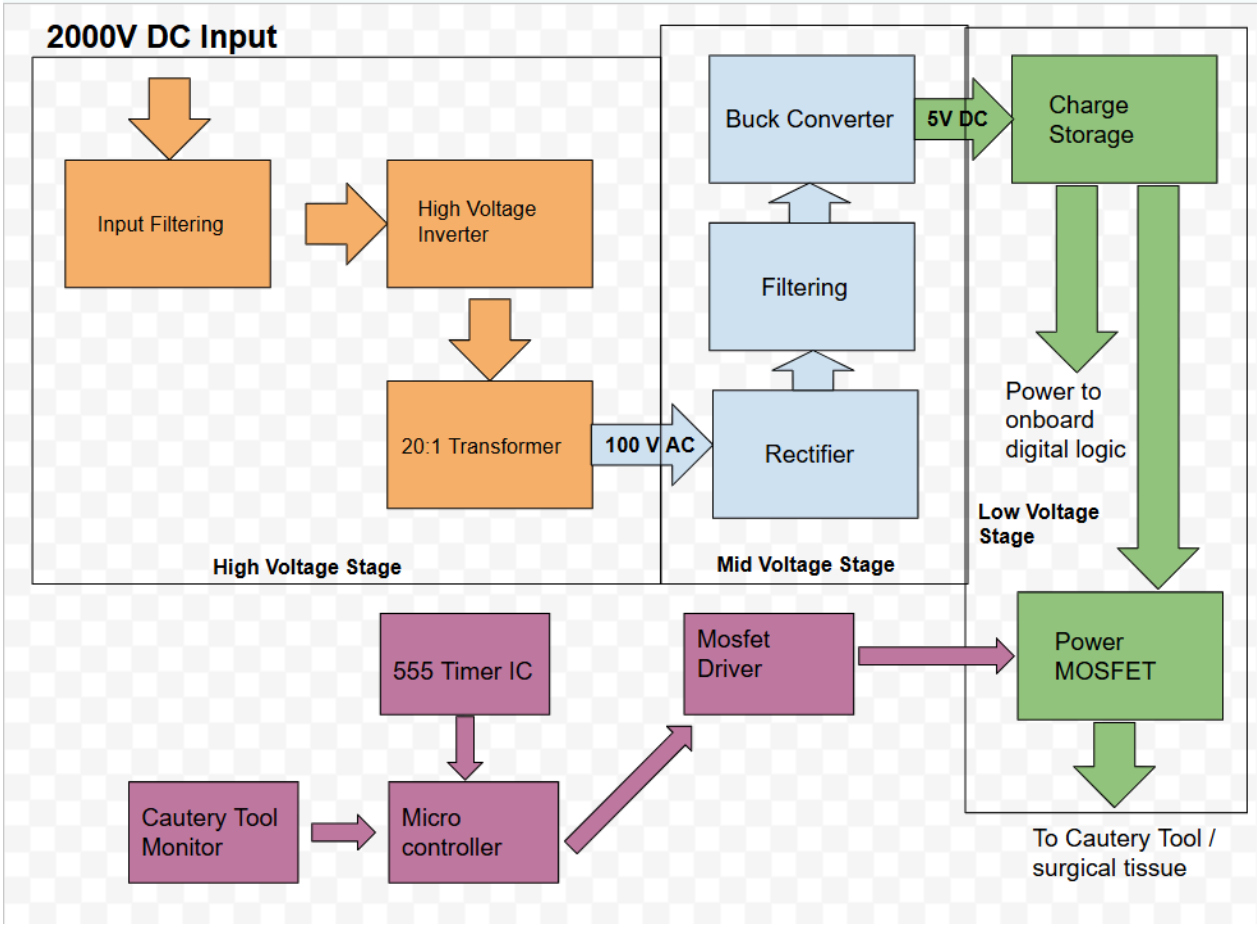

Figure 3: Block Diagram

The block diagram can be roughly divided into two main parts. The power section must safely and reliably step down 2000V to a 5V 100mA output. The signal section of this project must detect when the Cautery tool is in the off state, and then create a suitable nerve stimulatory waveform that will be outputted to the cautery tool through a power mosfet and driver circuitry.

2.2 System Overview

2.2.1 High Voltage Stage

A single stage buck is infeasible to safely and efficiently step down a 2000V DC input to a 5V DC output. We use 2000V DC as this is the output of the electrosurgical unit (ESU). Because of this, we will be implementing a multi stage power conversion system. The high voltage stage will take the 2kV DC and invert it to create a 2kV DC output. This will go through a transformer that will then step it down to 100V AC. This 100V AC will then be sent to a full bridge rectifier and filtering circuitry.

The preliminary design is centered around a Royer Oscillator, which is a type of relaxation oscillator. The royer oscillator is a self oscillating, push pull, AC/DC converter which uses a resonant LC circuit and the saturation of the transformer core to create an oscillatory AC output. It is widely used for low cost, low power DC to AC converters. There are a large number of advantages to using this type of circuit. As all the line and load regulation is done at the mid voltage stage, we do not need precise inverter circuitry on the high voltage inverter. Additionally, the entirely analog circuitry requires only the input power to run. Oftentimes inverters will need a low voltage rail to power the driver IC, which would not be feasible on our circuit. The most difficult part of this circuit is finding BJT's and a transformer that are properly rated for the oscillatory frequency and voltage. The design is based on the Masters Thesis of Scott McClusky from the California Polytechnic University, San Luis Obispo [5]. This output will then go to a 20:1 transformer to provide the mid voltage stage with the 100V AC it will use.

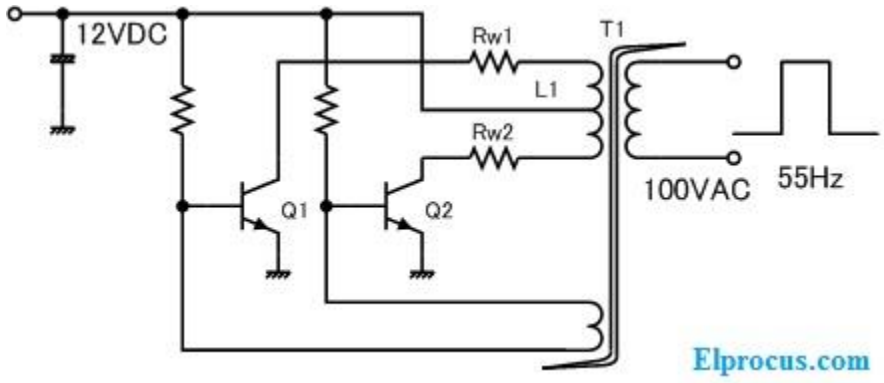

Fig 2.2.1.1: Circuit diagram of Royer Oscillator circuit

Significant considerations must be made when designing a PCB to handle multiple kilovolts. IPC 2221-b specifies design clearances, creepage, and dialectic breakdown for high voltage PCB designs. Additionally, the IEC 60601 specifies device tolerances and safety standards for any medical grade device. Another advantage of this design is the transformer provides isolation between the input and output, ensuring any malfunction on the high voltage side has no way to short through to the output of the neuroguard.

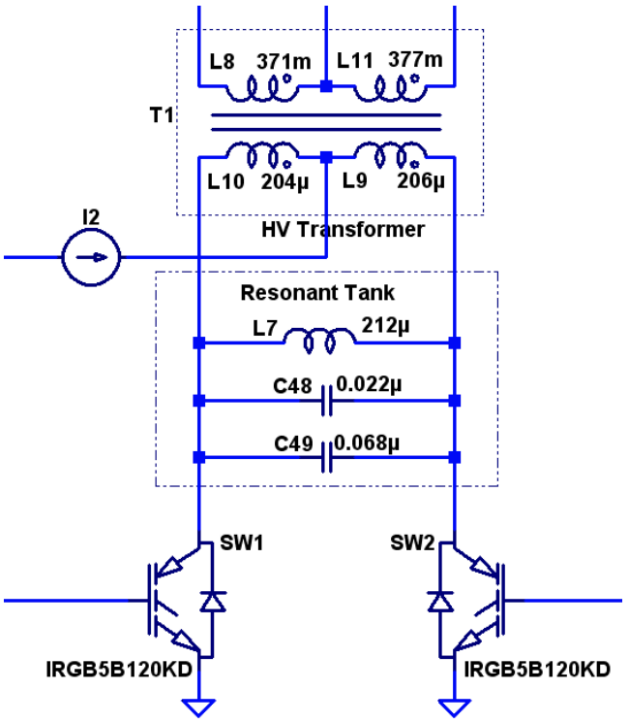

Fig 2.2.1.2: Another possible self resonant oscillator circuit. This topology utilizes a separate gate driver circuit. This is advantageous as it reduces the gate voltage compared to a normal Royer or Mizzolli self resonant circuit.

Requirement	**Measurement**
Output a stable 2000V AC output at 1kHz -	Output measurement on oscilloscope with

100kHz frequency	appropriate voltage shielding.
Meets all IPC2221-b and IEC60601 requirements for high voltage PCB design	Design rule check and verification in KiCAD or other design software.
No excessive distortion of input voltage source	Will require a specialized EMI measurement device.

2.2.2 Mid Voltage Stage

The Mid Voltage Stage contains the rectifier and filtering circuitry, as well as a final buck converter to do the final step down to 5V DC. This 100V AC input, once rectified and filtered, will output 100V DC that is then sent to a buck converter that will do the final step down to 5V DC. The Buck converter chosen for this task is the Texas Instruments LM5186. It is rated to a 120V input and capable of supplying a maximum of 300mA on the output. The synchronous buck converter features a variety of safety features, including over current protection, power good flag, soft start (to avoid start up transients), under voltage lockout protection, and redundant internal bandgap monitoring. Input to this is a full bridge rectifier composed of 4 BAV21W-7-F fast recovery diodes rated for 400mA and 200V each. A single 100 µF electrolytic capacitor is placed across this full bridge rectifier to smooth the output. A full schematic and detailed description of each subsection of this design is given below.

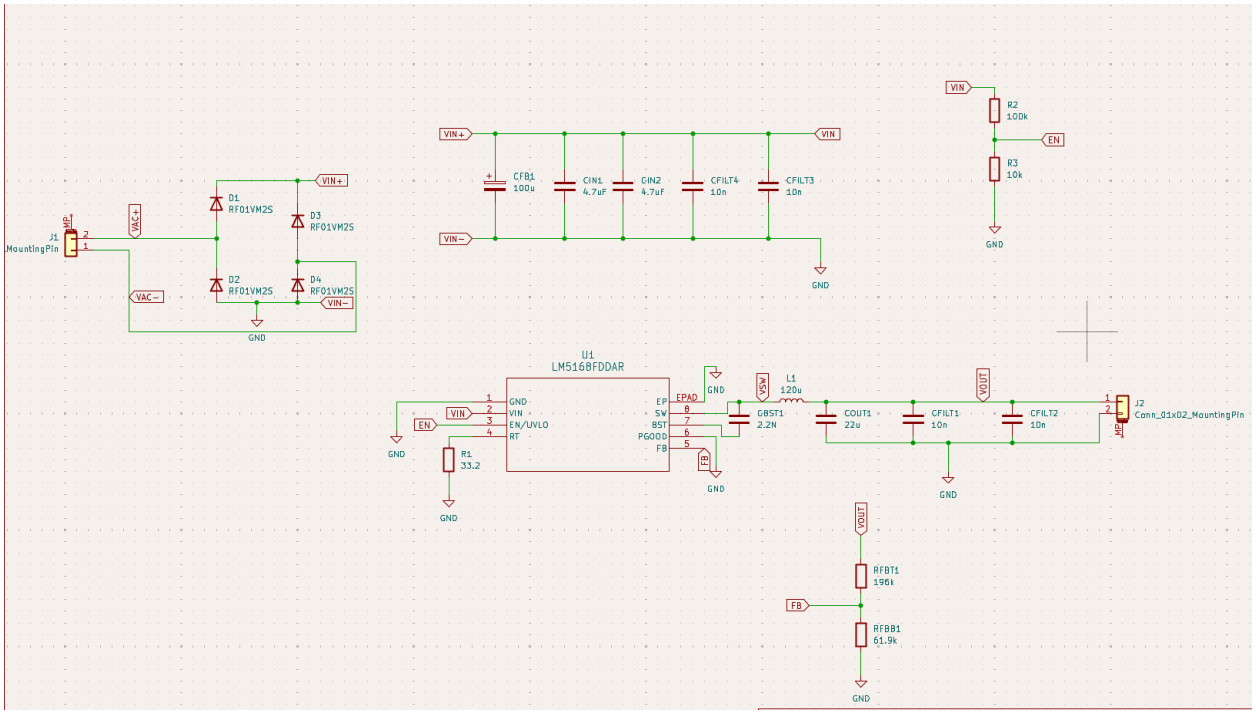

Fig 2.2.2.1: Schematic of Mid Voltage Step Down

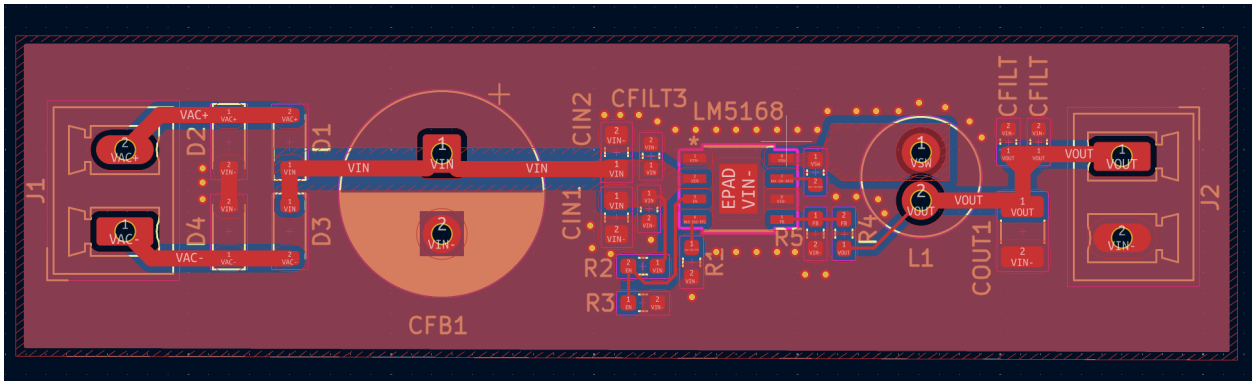

Fig 2.2.2.2: PCB Layout of Mid Voltage Step Down

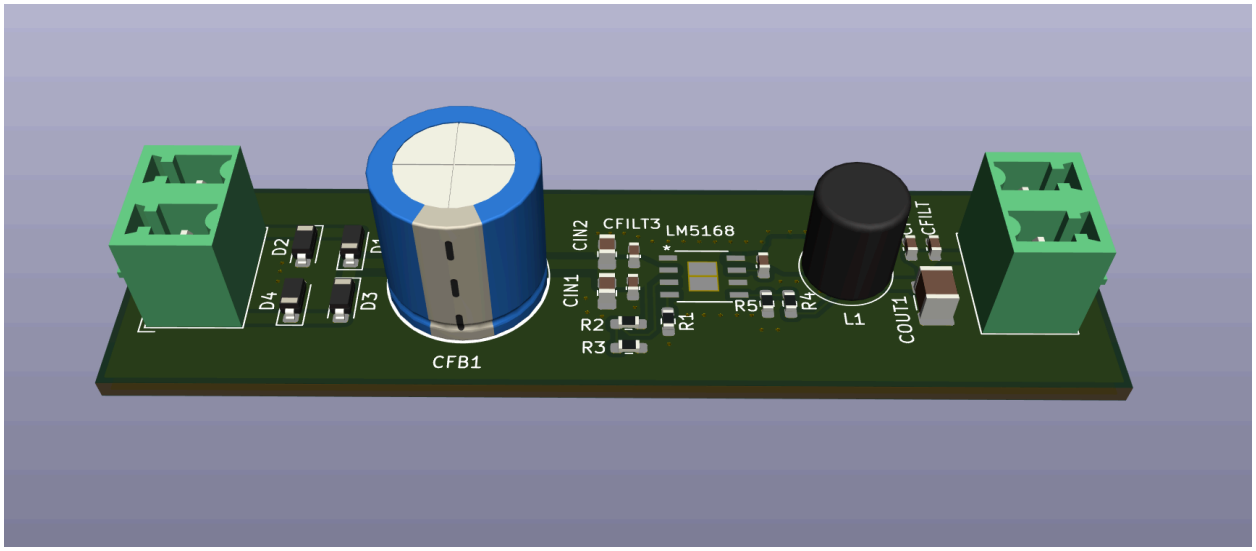

Fig 2.2.2.3: 3D Rendering of Mid Voltage Step Down

Buck Converter Layout and Design - Output Filtering

The output filtering is a crucial design element of the buck converter, and critical to its function. The inductor and output capacitors for this stage are sized appropriately to provide the necessary output current and minimal voltage ripple. These calculations were completed using formulas given from the Application and Implementation of the section of the LM5186 Data sheet [3]

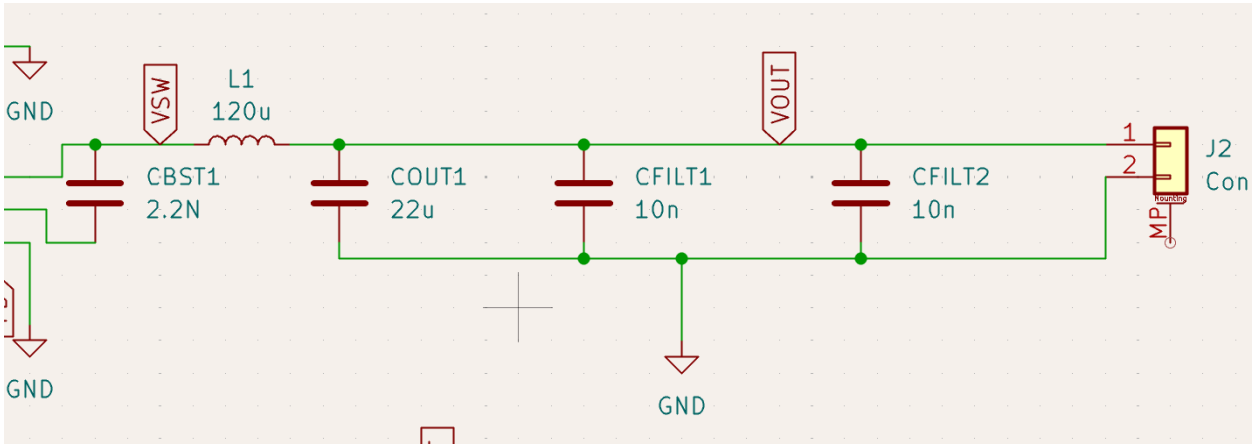

Fig 2.2.2.4: Output filtering of Mid Vin Stage

The Inductor and Capacitor (L1 and COUT1) were sized using the formula listed below. CFILT1 and CFILT2 are high frequency noise capacitors. While not contributing significantly to the power conversion of the buck converter, they give any high frequency noise (>1Mhz) a low

impedance path to ground, increasing the stability of the buck converter and mitigating any noise going to the output.

$$L = \frac{(V_{IN} - V_{OUT1})}{K \cdot I_{PRI} \cdot F_{SW}} \cdot \frac{V_{OUT1}}{V_{IN}}$$

Fig 2.2.2.5: Output Inductor Formula

$$C_{OUT} > \frac{I_{PK}^2 \cdot L}{2 \cdot V_{OUT1} \cdot \Delta V_O}$$

Fig 2.2.2.6: Output Capacitor Formula

These values were then calculated using Fsw = 750kHz, Vin =100V, Vout=5V, Ipri = 0.1A, Ipk = 0.3 A, and ΔVo = 0.5V. The switching frequency was chosen as 750kHz. This is lower than the devices maximum switching frequency, of 1000kHz, however due to the minimum on time of 50nS and our very low duty cycle, a lower frequency was chosen in order to avoid minimum time on constraints. This then gave an Rt value (timing resistor) value of 33.2 kΩ.

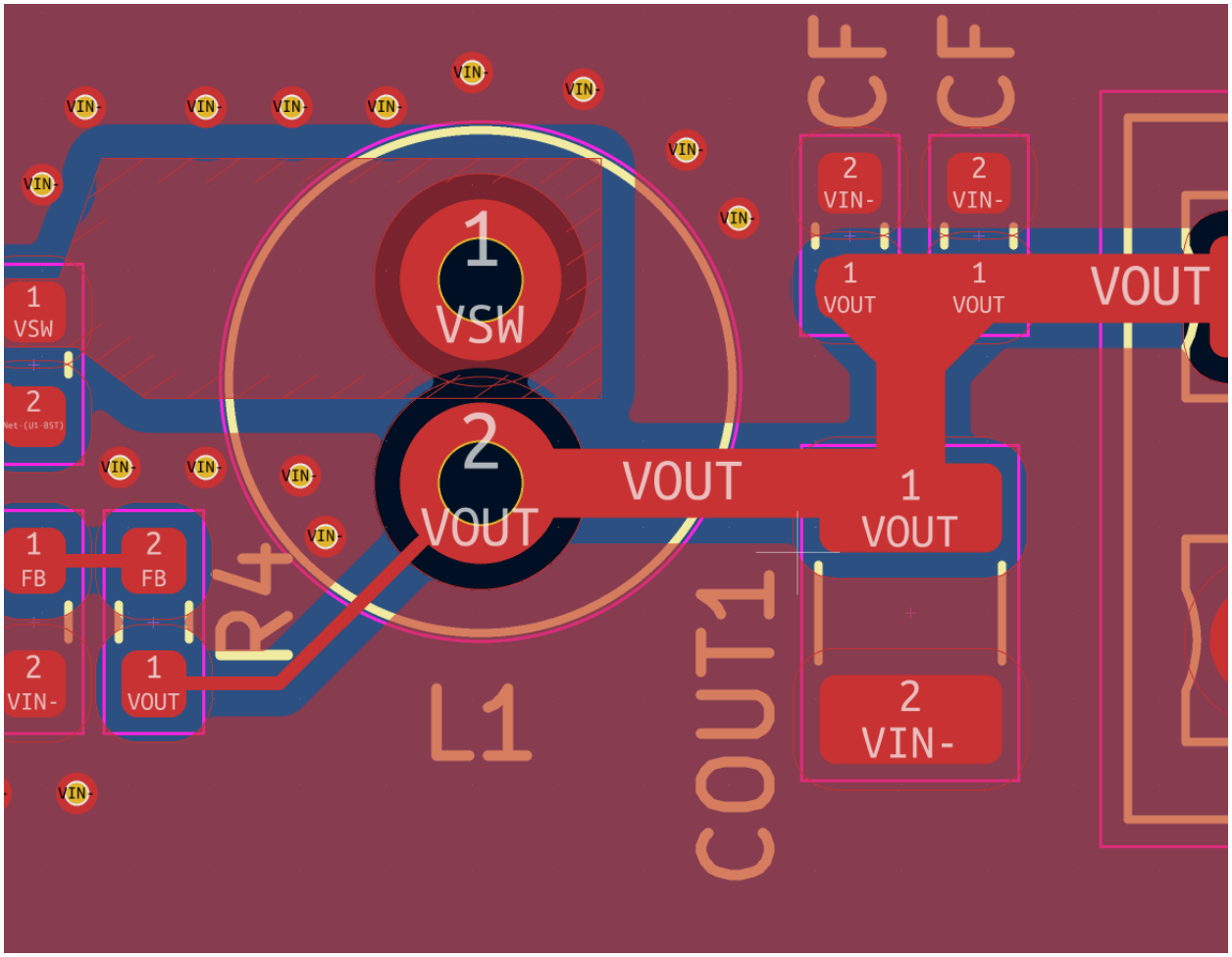

Fig 2.2.2.7: PCB Layout of Switch node and output Filtering.

Buck converters are inherently highly sensitive to PCB layout design. The high di/dt transients present at the output switch node (VSW) of a buck converter mean that any parasitic inductances in the PCB layout will create undesirable voltage spikes along the output. The switch node (VSW) is minimized as much as possible, and surrounded by ground Vias to aid with thermal dissipation and EMI protection. Clearances of 25 mil are maintained around the switch node to prevent arcing, in accordance with IPC-2221b clearance requirements [4], specifying a minimum of 0.5mm (19.3 mil), for a 100V external trace.

Buck Converter Layout and Design - Input Filtering and Enable Resistors

The Input filtering is critical to the buck converters function and integration into the wider power system. Buck converters will inherently draw a square wave type current, which can create voltage spikes from the parasitic inductances on the input line. Filtering capacitors are needed to smooth out this current to ensure integration with the wider electrical system, and provide charge for the current pulses that a buck converter will take in. A 100µF electrolytic capacitor is used to smooth out the pulsed DC from the full wave rectifier. This gives us a total input ripple to the buck converter of less than 2V. The inverter switching frequency will be selected to be significantly less than the buck switching frequency, such that the feedback loop on the buck can handle the voltage ripple on the input. The Enable resistor divider ensures that the buck will switch on only when it receives a suitable input voltage, in this case ~16V. This prevents the buck converter from trying to switch with an abnormal input, which could potentially cause damage to the device.

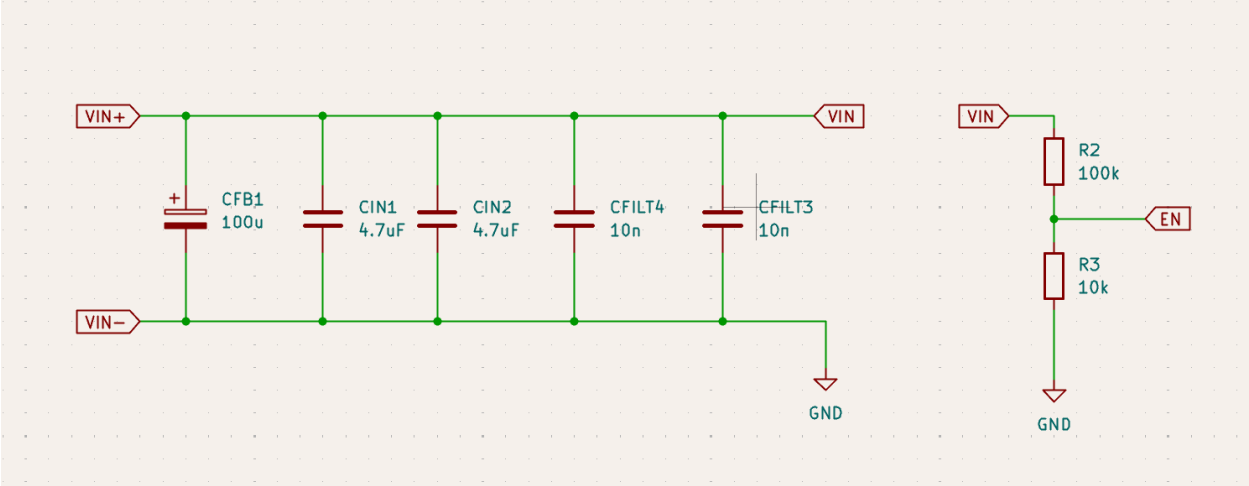

Fig 2.2.2.8: Buck converter Input Filtering and Enable Resistors

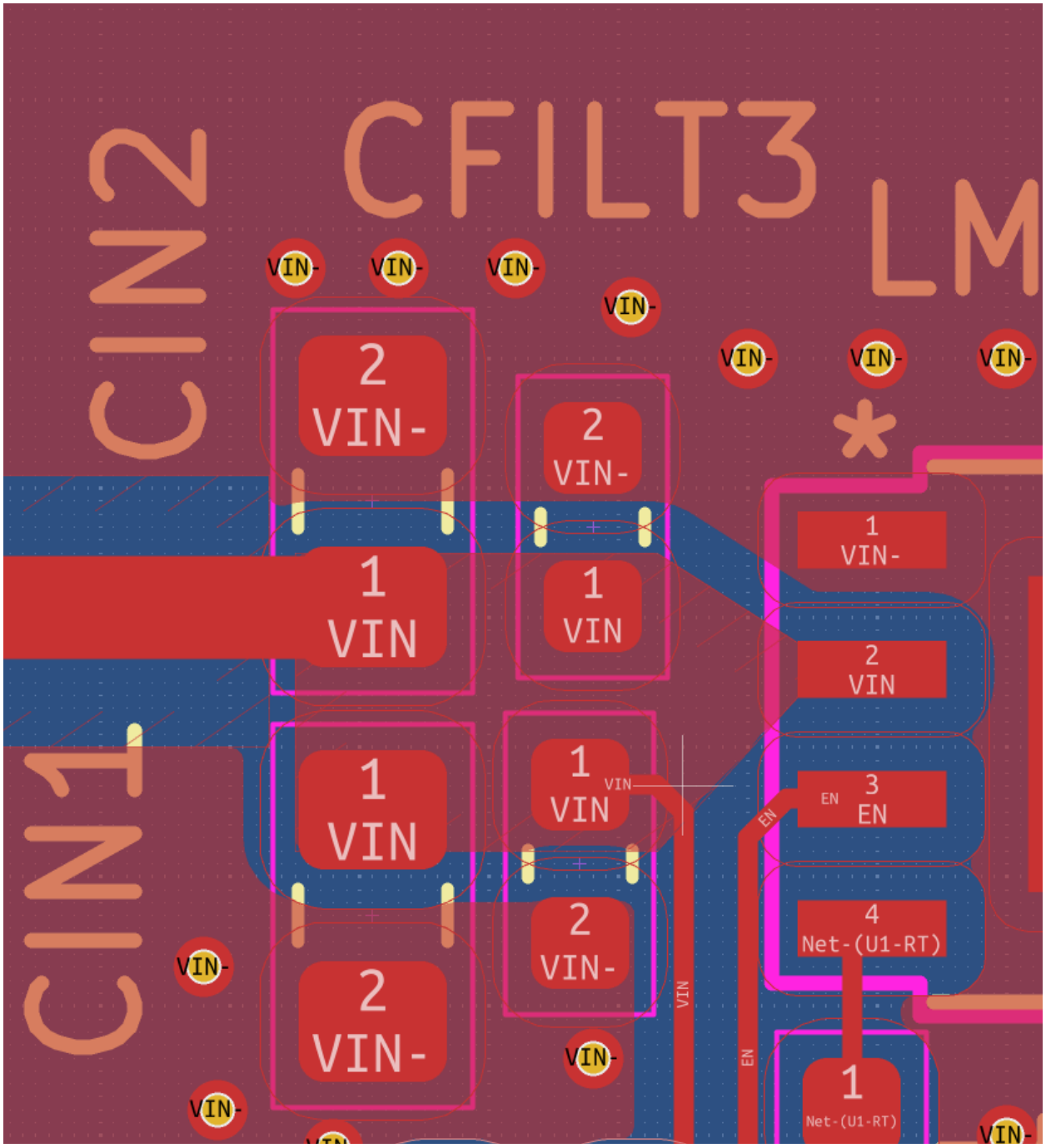

Fig 2.2.2.9: PCB Layout of input filtering capacitors (CIN1, CIN2, CFILT3, CFILT4).

The smaller input capacitors are sized at 4.7 µF for CIN1 and CIN2, and 10nF for CFILT3 and CFILT4. These capacitors are placed as close as possible to the input of the device to mitigate parasitic inductances, which would cause voltage spikes. The filtering capacitors are 10nF each, and similar to the output filtering capacitors, are in place to provide a low impedance path for

high frequency noise. These capacitors are all ceramic SMD packages, and are rated at 200V. This higher rating is necessary to avoid derating in the capacitors, which causes ceramic capacitors to become less effective at high voltages.

Buck converter Layout and Design - Feedback Loop

The feedback loop of a buck converter is incredibly important to help the converter maintain a stable output voltage and handle load transients appropriately. A simple voltage divider feedback loop is used here. If this design prevents insufficient stability during testing, then a feed forward capacitor (C ~50pF - 100pF), may be placed in parallel with RFBT to help with stability. The values of the feedback resistors were calculated from the formula below.

$$R_{FBT} = R_{FBB} \cdot \left(\frac{V_{OUT}}{V_{REF}} - 1 \right)$$

Fig 2.2.2.10: Feedback Formula

Here, V_{OUT} = 5V, and V_{REF} = 1.2V. There are an infinite number of possible combinations to use, but the design must take into account that higher resistances will increase efficiency, but make the feedback loop more susceptible to noise, and vice versa for a lower feedback resistance. To balance these considerations, a value of 196 kΩ was selected for R_{FBT}, and a value of 61.9kΩ was selected for R_{FBB}. The PCB layout is given below. It is important to ensure that the output of the feedback resistor is placed as close to the FB pin of the IC as possible to avoid noise coupling. Additionally the Vout line to the feedback is kept as short as possible and ground vias are placed in between the feedback resistors and the switch node, again to prevent noise coupling.

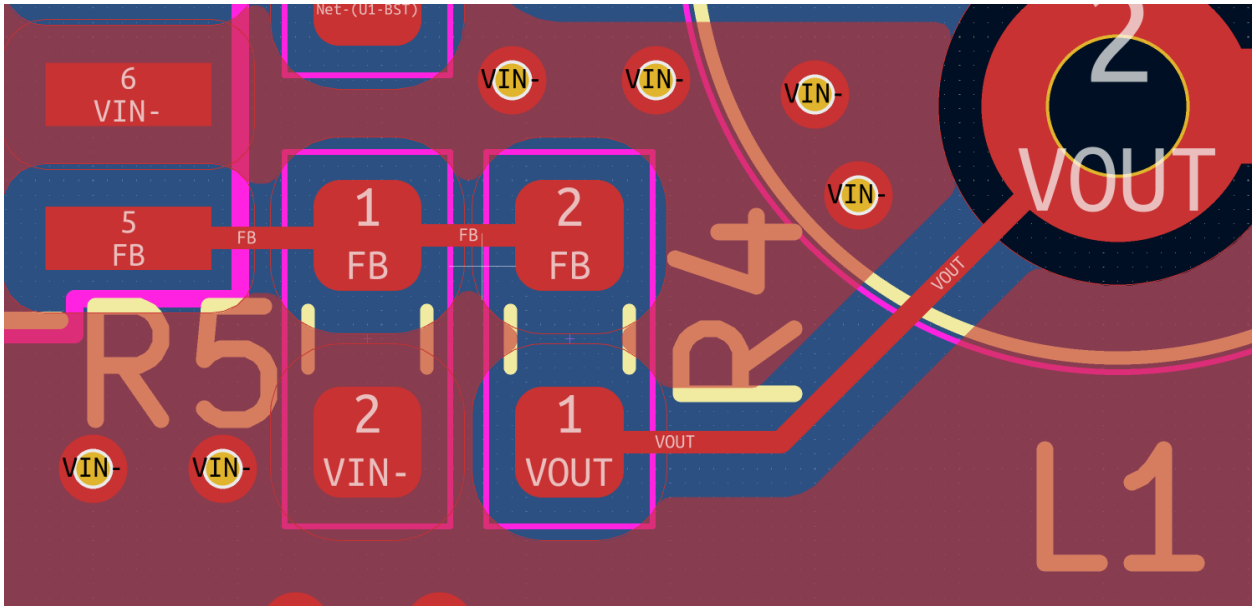

Fig 2.2.2.11: Feedback Resistor Layout.

Buck converter Layout and Design - Thermal and EMI considerations.

Despite being a relatively low power design (0.5W), and operating at moderate efficiency (~60%), this buck will still require the dissipation of a non-negligible amount of power. The PCB is designed to allow high thermal conduction from the IC to the board, and then from the board to the ambient environment. The board is designed with unobstructed ground planes above and below to allow for efficient heat dissipation. Additionally, the ground vias on top and below the board allow heat to effectively conduct to the bottom ground plane, where it then can be more easily dissipated. An IC package with a large copper pad on the bottom of the device is connected to the ground plane to allow for better heat dissipation as well.

As buck converters are inherently noisy components, EMI (Electromagnetic Interference) must be accounted for in the schematic and PCB layout. A large amount of ground vias are placed around the device and the switch node to prevent conducted noise along the ground plane. If there is excessive distortion of the input supply, an EMI filter may be added in between the full bridge rectifier and filtering capacitors to suppress this.

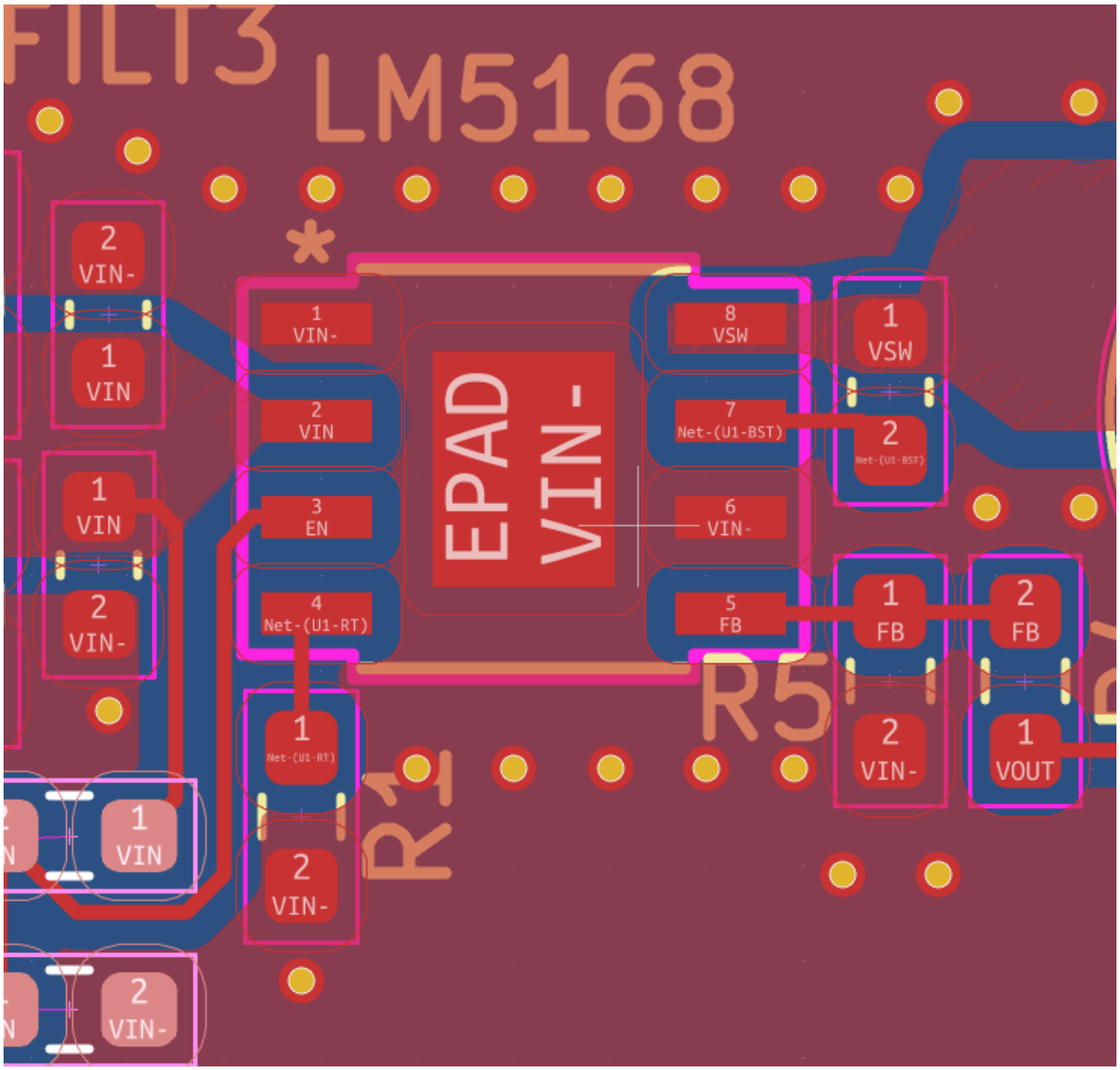

Fig 2.2.2.12: Thermal and EMI considerations around the conductor.

Buck converter Layout and Design - Simulation, Testing, and Verification.

This design was simulated in PSpice for TI (whose simulation software comes from Cadence), and performed well. A result of the simulation is shown below. The Red trace is enable voltage, the green trace is output voltage, the dark blue trace is input voltage, the yellow trace is feedback voltage, and the cyan trace is inductor current. This shows stable operation with a nominal output voltage of 5V and minimal voltage ripple.

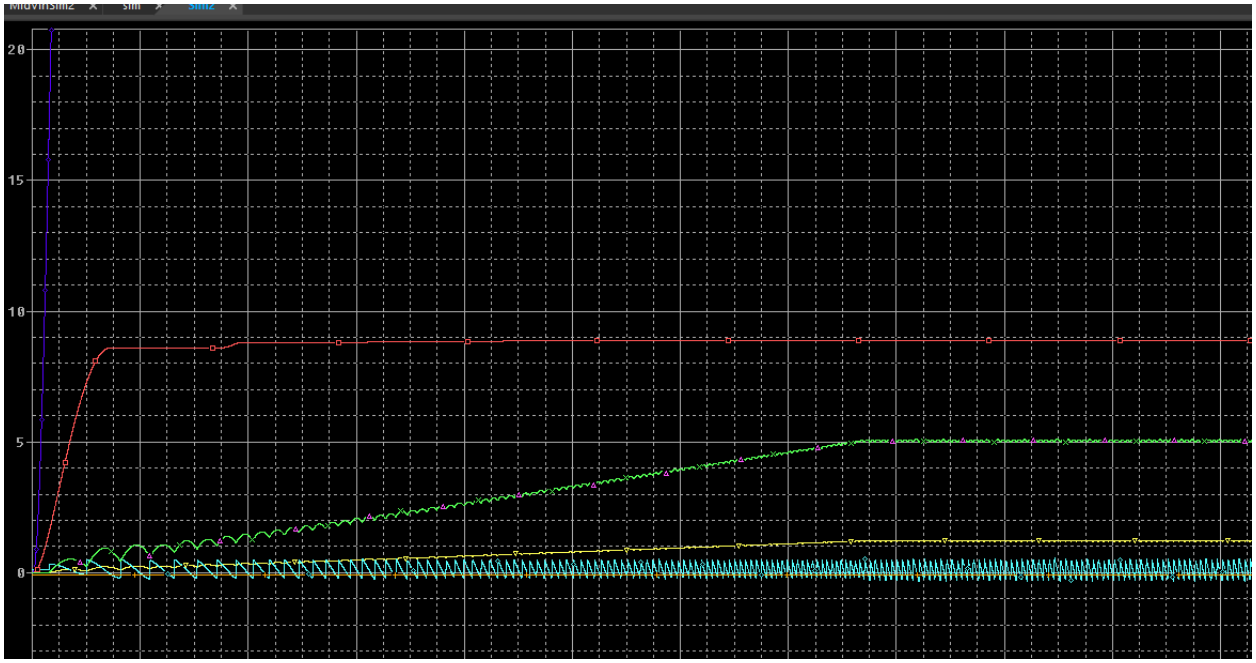

Fig 2.2.2.13: Cadence simulation of Buck converter and rectifier.

Listed below are the performance criteria for this design, and the method of verification.

Requirement	**Verification**
Buck converter outputs 5V at 100mA, output voltage ripple is less than 0.25V	Oscilloscope measurement of output voltage with resistive load of 50Ω. Input power will be from Variac. Input will start at 30V AC and increment to 100V AC once safe device behavior is confirmed.
Full bridge rectifier archives output DC voltage of 100V @5% with voltage ripple less than 2V	Oscilloscope measurement of Vin trace

Buck converter can handle 100mA to 300mA output transient in <10 uS.	Oscilloscope measurement of Vout with electronic load.

2.2.3 Timer & Low Voltage Stage

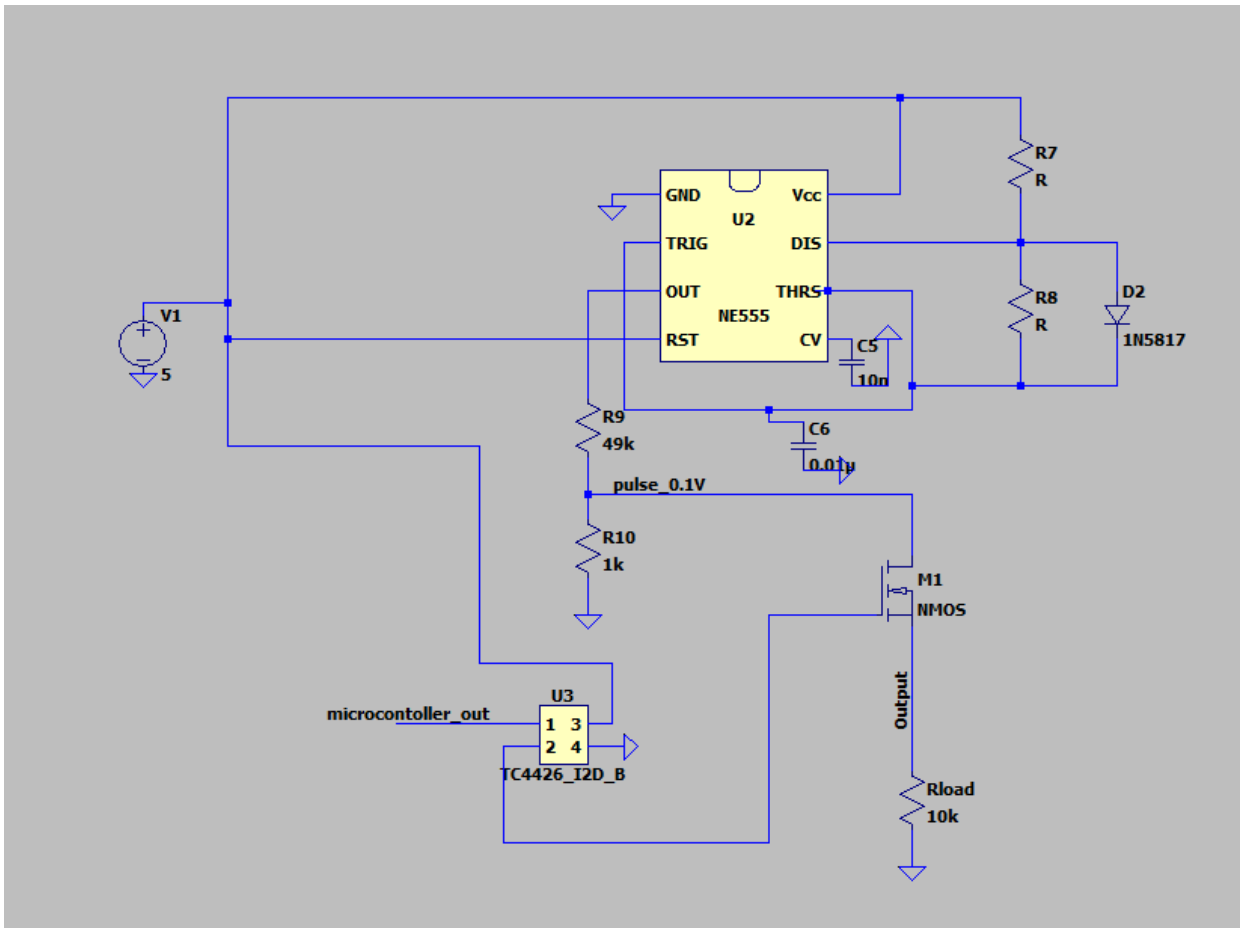

Fig 2.2.3: Low Voltage Stage Circuit.

The input being the 5V DC from the mid-voltage stage, a 555 timer IC is used to generate a 0.1V 50-1kHz signal, with a pulse width 100us - 1ms. This is selectively discharged through a resistor (simulating nerve tissue) via an N-channel MOSFET, whose gate is driven by a 5V pulse signal from the microcontroller via a gate driver. When the gate receives a high signal, the MOSFET turns on, allowing the capacitor to release its energy as a precise stimulation pulse across the load.

R7 and R8 to create a 0.1V, 1kHz, 100 µs pulse signal can be chosen to be R7 = 15kOhms, R8 = 130kOhms.common NE555) uses different formulas depending on its operating mode: for astable mode, the formulas are: *tHIGH*=0.693(*RA*+*RB*)*C*, *tLOW*=0.693(*RB*)*C*, T = *tHIGH* + *TLOW*.

Requirements	Verifications
1. The signal at pulse_0.1V is measured to be 0.1V, outputting at the frequency desired between 50Hz-1kHz, and a pulse width between 100us - 1ms.	● Probe pulse 0.1V using a multimeter ● Confirm multimeter matches simulation waveform/breadboard results and is measured between the requirements listed.
2. Confirm output is only high when mircocontoller_out is high	● Probe Rload and microcontroller_out. ● Confirm 0V is measured when microcontoller out is low, and a pulse signal is measured when it is high.

2.2.4 ESU Monitor & Microcontroller Stage

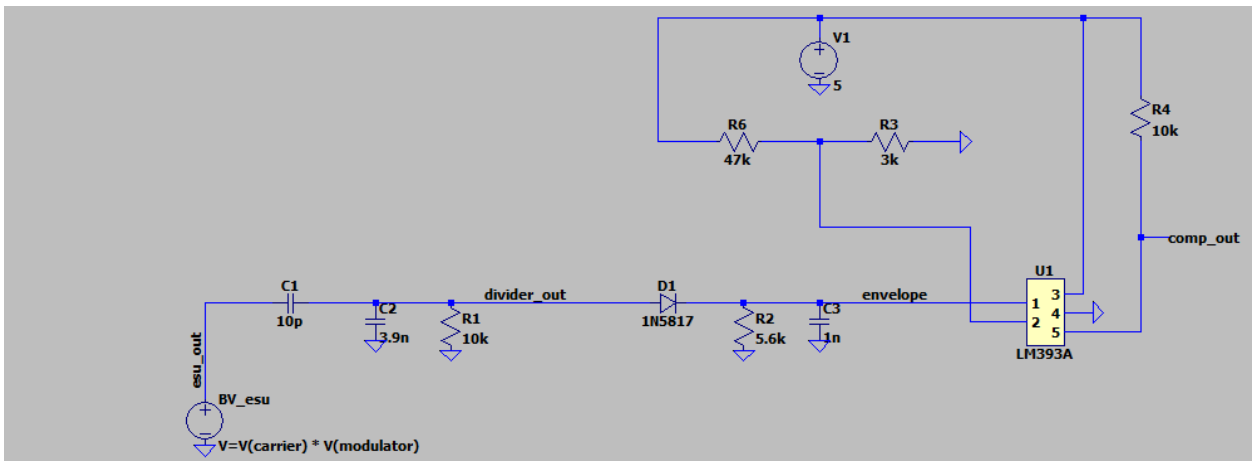

Fig 2.2.4: ESU Monitor Circuit.

The microcontroller detects when to alternate between the standard cautery function

(pass-through) and the nerve stimulation waveform. The ESU source is the input, which is a 2000V AC source with a 357-500 kHz, and a Duty Cycle from 5-75%. It also takes as input the 5V DC from the low voltage stage and uses it to create a Vref of 0.3V in the LM393 comparator. This PCB provides the Cautery Tool Monitoring, which detects the ON and OFF duty cycles of the ESU source via a capacitive voltage divider that feeds into an envelope detector, and to the comparator in order to detect the OFF periods of duty cycle of the ESU, which is when the nerve stimulation is allowed to be delivered. Comp_out is the input to the microcontroller, which outputs a HIGH signal when the comp_out is LOW and vice-versa. This will output a signal to the mosfet driver from section 2.3.3 that when high (5V), will turn MOSFET turns on, allowing the stimulation pulse across the load during the OFF cycles.

C1 and C2: The division ratio is approximately C1 / (C1 + C2). Ratio ≈ 10pF / (10pF + 3900pF) = 10 / 3910 ≈ 1/391 This reduces the peak voltage from 1850 to 2000V down to a much more usable 4.7V - 5V AC.

R2 and C3: These components create the crucial RC time constant (τ). $\tau = R * C = 5{,}600\ \Omega * 0.000000001\ F = 5.6\ \mu s$. It must be longer than the carrier period, and the carrier period at its lowest is 1 / 307kHz ≈ 3.26 µs from ESU manual [6]. The 5.6 µs is long enough that C3 does not discharge between peaks.

Requirements	**Verifications**
1. The peak V(divider_out) is measured to be below 10V and the positive peak greater than 0.5V, which is more than the 0.3V threshold needed by the comparator.	● Probe test divider_out using a multimeter ● Confirm multimeter matches simulation waveform/breadboard results and is measured between the requirements listed.

2. The diode properly acts as a half-wave rectifier and outputs a signal matching the output of V(divider_out)	● Probe test points of envelope with multimeter ● Confirm the maximum voltage is between below 10V and the positive peak greater than 0.5V, which is more than the 0.3V threshold needed by the comparator.
3. The Vref of the comparator is measured to be 0.3V with 5% tolerance. The output of the comparator is measured to be 3.3V when the input envelope detector is above 0.3V and 0V when below.	● Probe inputs and outputs of comparator with multimeter. ● Confirm Vref is input voltage is correct

2.3 Subsystem Requirements

2.3.1 High Voltage Stage

Power supply can successfully output 100V AC 5% tolerance. The entire apparatus is safe to use under medical criteria.

2.3.2 Mid Voltage Stage

Power supply can successfully output 5V DC 5% tolerance at 100mA 5% tolerance with voltage ripple less than 10% (Output supply maximum ripple is from 4.5V to 5.5V, DC output is maintained from 4.75V to 5.25V). The entire apparatus is safe to use under medical criteria.

2.3.3 Low Voltage Stage

When the Mosfet receives a high signal, the MOSFET turns on, allowing the capacitor to release its energy as a precise stimulation pulse across the load is measured to be 0.1V at 50 Hz - 1 kHz. The waveform generated during the OFF period is still the ESU source.

2.3.4 ESU Monitor & Microcontroller Stage

The microcontroller, given a 5V input with a certain % Duty Cycle, is able to time when nerve stimulation occurs. The microcontroller must output 5V to the Mosfet Driver during the OFF portion of the Duty Cycle, and according to the 555 timer.

2.4 Tolerance Analysis

Significant considerations must be taken on the PCB layout and design for this power system. High voltage DC will require larger trace tolerances and specialized PCB dielectric to prevent arcing between traces. This entire apparatus must then be placed into an insulating chamber for improved safety. While buck converters are generally the most efficient method to step down DC voltages, because of the large jump from input voltage to output voltage required (100V DC to 5 V DC), efficiency will be closer to ~50% depending on the specific buck converter chosen. Thermal considerations are incredibly important so the buck converter does not overheat and shut down. The final large consideration is EMI filtering from the buck converter and Inverter sub systems. The DC power supply NeuroGuard will receive is incredibly sensitive to backpropagated conducted EMI. Significant filtering will need to be in place in order to ensure that this does not disrupt the cautery power supply.

3.1 Cost Analysis

Low Voltage and Microcontroller Part and Cost Analysis

Below is the table of parts used in the low voltage and microcontroller part of the circuit, and their respective cost. The exact cost is of the basic components used, more parts were used for testing and redundancy purposes. The majority of parts in these subsystems were acquired from the ECE supply center for free, but the unit cost is still provided.

Part Number	Description	Quantity	Cost (USD) $
296-6501-2-ND	IC OSC SGL TIMER 100KHZ 8-SOIC	1	0.28
TC4426ACPA	IC GATE DRVR LOW-SIDE 8DIP	1	1.54

CPF0805B49K9E	49 kΩ, 0.1% resistor, 0603	1	0.1
RT0402BRD0715KL	15 kOhms 0.1% resistor, 0.063W	1	0.1
RG2012P-102-B-T5	1 kΩ, 0.1% resistor, 0603	1	0.1
ERA-2AEB103X	10 kΩ, 0.1% resistor, 0603	3	0.3
CC0402KRX7R9BB103	0.1μF, 50 V, 0402	2	0.16
1N5817	DIODE SCHOTTKY 20V 1A	2	0.18
DMPH16M1UPSW-13	12V N-MOS 12-V, Surface Mount	1	0.32
0603N100J500CT	10 pF, 50V Ceramic Capacitor, 0603	1	0.1
GRM155R71H392JA01D	3.9 nF, 50V Ceramic Capacitor, 0603	1	0.1
CL21B102KBANNNC	1 nF, 50V, Ceramic Capacitor, 0805	1	0.1
RMCF0603FT3K00	3 kΩ, 1% resistor, 0603	1	0.1
RMCF0603FT5K60	5.6 kΩ, 1% resistor, 0603	1	0.1
RMCF0603FT47K0	47 kΩ, 1% resistor, 0603	1	0.1
LM393ADR	Comparator (General Purpose) Open-Collector	1	0.37
STM32F401RBT6	IC MCU 32BIT 128KB FLASH	1	4.96
PCB Order	PCB	1	0.5
Labour	Cost of Labour ($15/hour)	3 hour	45
Total	—		54.512

Mid Voltage Part and Cost Analysis

Below is a table of parts, and their respective cost for the mid voltage source. As this is dealing with specialized high voltage components, the cost is significantly higher than what would be expected for the same low voltage component. As additional parts were ordered for redundancy

and testing purposes, the exact cost of the project does not precisely reflect this spreadsheet.

Part Number	Description	Quantity	Cost (USD) $
BAV21W-7-F	200 V, 400 mA small-signal diode, SMD, SOD-123	4	0.4
OSTTC022162	2-position screw terminal block, 5.08 mm pitch	2	1.14
EKMQ161ELL101MK25S	100 µF, 160 V radial electrolytic capacitor	1	1.13
C2012X5R2A475K125AC	4.7 µF, 100 V, 0805 MLCC capacitor	2	1.5
C0603C103K2RECTU	0.01 µF (10 nF), 200 V, 0603 MLCC	4	0.6
RC0603FR-07100KL	100 kΩ, 1% resistor, 0603	1	0.1
RC0603FR-0710KL	10 kΩ, 1% resistor, 0603	1	0.1
RC0603JR-070RL	0 Ω jumper resistor, 0603	1	0.00292
RLB0712-121KL	120 µH radial inductor	1	0.28
C0603C222J2GACTU	2,200 pF, 200 V, 0603 MLCC	1	0.01974
CRCW060333K2FKEAC	33.3 kΩ, 1% resistor, 0603	1	0.1
CL32A226KAJNNNE	22 µF, 25 V, 1210 MLCC	1	0.14376
C0603C103K5RACTU	10 nF, 50 V, 0603 MLCC	2	0.16
RC0603FR-07196KL	196 kΩ, 1% resistor, 0603	1	0.1
CR0603-FX-6192ELF	61.9 kΩ, 1% resistor, 0603	1	0.1
LM5168	120V 0.1A Synchronous buck convert	1	3.77
CMF5550R000FKEK70	50 Ω ±1% metal film resistor (through-hole)	1	0.56
PCB Order	PCB	1	0.5
Labour	Cost of Labour ($15/hour)	3 hour	45
Total	—		55.70642

Cost Analysis for High Voltage Section.

The design of the high voltage section has not been finalized, and thus an exact value cannot be given. Based on the circuit design, a rough estimate can be provided. The high voltage BJT will be about $4 for two. High voltage capacitors and resistors will total to approximately $10. A specialized high voltage transformer will cost anywhere from $10 - $20. While a specialized high voltage PCB and enclosure may cost anywhere between $20 and $40. This will bring the total cost for this section of the design to $50 for a conservative estimate and $100 in a worse case scenario.

Labor Cost

Team Member	$/hr	Total Hours	Cost (USD) $
Stephen	$40	10hrs per week for 14 weeks	$5,600
Aidan	$40	10hrs per week for 14 weeks	$5,600
Alex	$40	10hrs per week for 14 weeks	$5,600

3.2 Schedule

Week of	Task	Group Member(s)
10/13	Finalize Low Voltage/Microcontroller Design Draft PCB in KiCAD Second Round PCBway Order (Low Voltage)	Alex, Stephen Alex All
10/20	Microcontroller Selection Assemble First PCB	Alex Aidan

	Program Cauterizing Detection Prepare for Breadboard Demo	Stephan All
10/27	Finalize GPIO Pin Configurations Finalize High Voltage Design Breadboard Demo 2	Stephan Aidan All
11/3	Assemble Second PCB Test First PCB Order High Voltage PCB	Stephan Alex Aidan
11/10	Test Second PCB Integrate Different Voltage Systems Assemble & Test High Voltage PCB Order Final PCB (If Necessary)	Alex All Stephen Aidan
11/17	Mock Demo Team Contract Assessment Test System Integration Start on Final Report and Presentation	All All All All
11/24	Fall Break Finalize Presentation and Report	 All
12/1	Final Demo Mock Presentation Work on Final Report	All All All
12/8	Final Presentation Final Paper Due Lab Notebook Due	All All All

4 Ethics & Safety

To make sure our group is working on our project safely and effectively, we will follow the IEEE Code of Ethics that was adopted by the IEEE Board of Directors in 2020[2]. We understand that

technologies affect the quality of life around the world and we must work with a high ethical standard as a professional team. Some of the most important, but not the only, ethics to follow for our team are:

1. **Seek, accept, and offer honest criticism of technical work, acknowledge and correct errors, be honest, and realistic in stating claims or estimates based on available data [2].**

   It is important to work as a team to keep an open mind that we will not accomplish every part of our project perfectly right away. During our TA meetings, we will be able to receive feedback, positives or criticisms, to improve on our project. In our lab notebook, we will take note of all our progress and data, along with what we discussed in TA meetings, to provide a basis for our project claims.

2. **Treat all persons fairly and with respect, to avoid harassment or discrimination, and to avoid injuring others [2].**

   As we work throughout the project, we will spend time together and apart to create the final product. When we work together, we must listen to each other and consider every one's opinions in a discussion about our project. Everyone's opinion needs to be considered for there to be a fair decision-making process.

3. **Work to improve our technical competence but consider our qualification from training or experience and disclose notable limitations [2].**

   Since completing our proposal document and review, all members of the team have completed the soldering and KiCAD assignment which builds a basic understanding for designing our PCBs. Also, we have met with the Neuroguard Carle Medical team to understand their design aspirations and how to adapt our design with the cauterizing

machine. As we continue the project, we will continue to expand our knowledge as more questions arise during our implementation.

4.1 Risk Analysis

To ensure safety in our design and following all regulations, we will take a number of precautions to minimize danger in development and operation of our device. Because we will be dealing with high voltage, possibly of 2000 Volts if connected to the hospital supply, it is important to make sure all components included in our design can withstand these voltage levels, even after step-down converters are included. Again, because this is a project dealing with high voltage, we will create a Safety Manual and demonstrate that our project complies with the safety manual at the time of demo.

Another risk to consider is the large losses that can be found in our electrical system. Because we are dealing with high voltage, these losses can generate lots of heat which can be dangerous for the device and the user. Therefore, we will make sure all components in the device operate at a temperature under its rating and use ventilation tools, as required. Also, we will make sure that all devices, such as microcontrollers, and software follow relevant licensing requirements.

5 References

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