Neuroguard: A Dual Electrocautery-Nerve Monitoring Device to Prevent Injury During Mastectomy

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Abstract

Post-mastectomy pain is a common element of the patient experience in the weeks and months following surgery. The majority of cases have been attributed to transection of the intercostobrachial nerve (ICBN), a cutaneous nerve that provides sensation to the chest wall and upper arm. With reconstructive surgeries and allografts posing their own set of potential complications, exploring avenues for preventing nerve injury within the operating room can pave the way for safer procedures that maximize patient outcomes. By redesigning the way a standard electrosurgical unit (ESU) delivers energy to tissue, we propose a novel tool for intraoperative neuromonitoring (IONM) that can be integrated within existing surgical workflows. This work is a proof of concept for the hardware platform, demonstrating the capability to integrate power conversion and waveform generation that could be implemented with a standard cautery probe.

Contents

1. Introduction

Over 100,000 mastectomies are performed yearly in the U.S., with 40-60% resulting in nerve injury that can lead to a variety of symptoms, notably post-surgical pain [1]. In particular, damage to the intercostobrachial nerve (ICBN) is common during mastectomy and axillary lymph node dissection, a set of procedures common in treating metastatic breast cancer. Recently, surgeons have begun utilizing nerve-sparing techniques to ensure greater patient quality of life; however, these innovative techniques require meticulous dissection that can be complicated by anatomical variation and intraoperative bleeding.This highlights an urgent need for a device that provides real-time feedback to surgeons, enhancing safety and precision while also being easily integrated into existing workflows. To address this problem, we propose NeuroGuard, a device designed to alert surgeons when they are approaching the ICBN nerve during operations, thereby reducing nerve injury rates and improving patient outcomes.

Inspired by recent multifunctional surgical devices like a dual monopolar probe and suction tool, we are working with the NeuroGuard team to integrate contactless nerve detection and cautery functionalities into a single, cost-effective device. Over the course of the semester, we will work to design and simulate a circuit that demonstrates the ability to switch between predefined electrocautery and nerve stimulation waveforms at specified time intervals. We will work to prototype this circuit that can be integrated with an electrosurgical unit and standard monopolar electrocautery probe. This project is a proof of concept for the hardware platform, demonstrating the capability to integrate power conversion and waveform generation that could be used with a standard cautery probe. The scope is strictly limited to the development and testing of this hardware; the detection of neural activation and the development of a feedback mechanism are considered future work beyond the scope of this project.

2 Design Overview

The design of the neuroguard must satisfy a few key objectives. Power supply integration with the output of an Electrosurgical Unit (ESU), detection of the ESU operation state, and creation of suitable nervous stimulatory waveforms. This nerve stimulation waveform is sent out as a pulse signal during the OFF portion of the duty cycle of the electrocautery AC source and Neuroguard is powered by this same source. The specifications of what the nerve stimulation signal should be, and the input source were specified by the medical team [3], and the actual detection of nerves using this circuit is a next step outside the scope of this project. The block diagram in Figure 1 shows each section of the design and how they connect together.

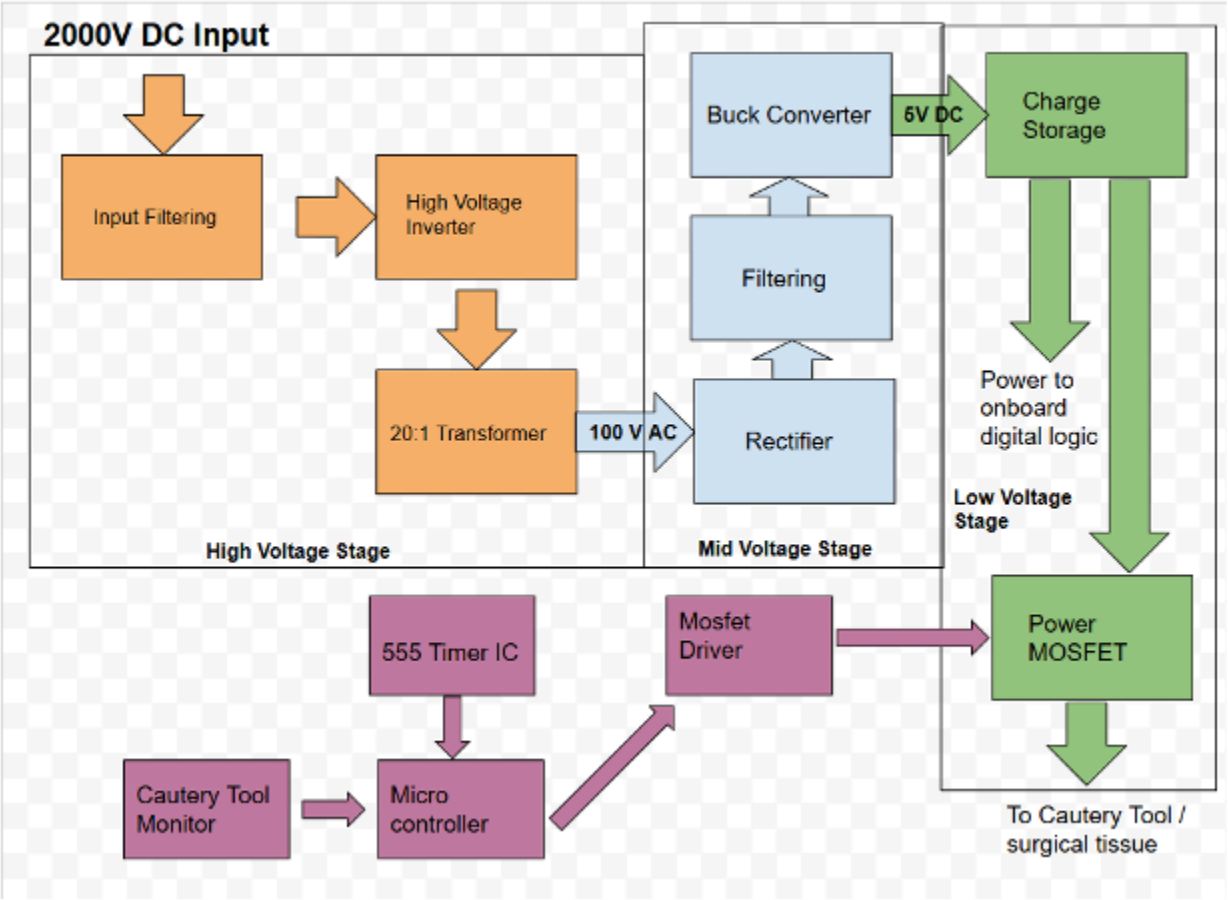


Figure 1: Block Diagram for Design

2.1 Power System

One of the key aspirations, and challenges, of the neuroguard, is to be able to integrate directly with the output of an ESU. This includes being able to power the device directly from the output of the ESU. The reason for this is to increase ease of use for practitioners, allowing for one apparatus that can connect in between the ESU output and cautery pen. Additionally, having a separate power supply for the device would make it more expensive and regulatorally complicated, hindering the use and uptake of the device. The power system of neuroguard must therefore be able to use the output of an ESU, and safely

step down the device to 5V, for use in the low voltage circuitry and creation of suitable nervous-stimulatory waveforms.

2.1.1 High Voltage

One of the key challenges for this design project was the high voltage work. The Bovie Electrosurgical Generator, the cautery machine that the neuroguard is being designed for, produces maximum open circuit voltages in monopolar mode between 1250V- 3900V [2], with peak voltages being even higher The differential oscilloscope probes, which are the highest rated voltage measurement equipment that students have access to, has a maximum voltage of 1500 V. This makes it difficult to even get a measurement of the output in the first place without risking damage to expensive school equipment. School research labs have equipment rated for higher voltages, but these require tedious logistical setups and consent from the supervising professor. Additionally, safety concerns are at the paramount of this course. An output of 1500V at 70W is easily capable of causing permanent injury and death to students. Because of all these concerns, ultimately high voltage work fell out of the scope of the project for this semester.

Nonetheless, through the research we have done this semester, we have proposed a design to be tested by the neuroguard team that allows for the implementation of a high voltage power source from the ESU. From reading the Bovie Electrosurgical Generator patent, it was noted that when not operating, the device outputs a 'quiescent voltage' across its monopolar outputs. This voltage could be used by the neuroguard to draw power from the ESU when the device is off, through a step down transformer. When the neuroguard detects that the ESU is on and outputting a higher voltage cutting or coagulating waveform, the power supply would use a high voltage e-fuse to disconnect itself from the output, in order to prevent interfering with the surgical operation of the ESU. Again full measurements and characterization of the ESU output are needed to begin formal design, construction, and testing of this proposal.

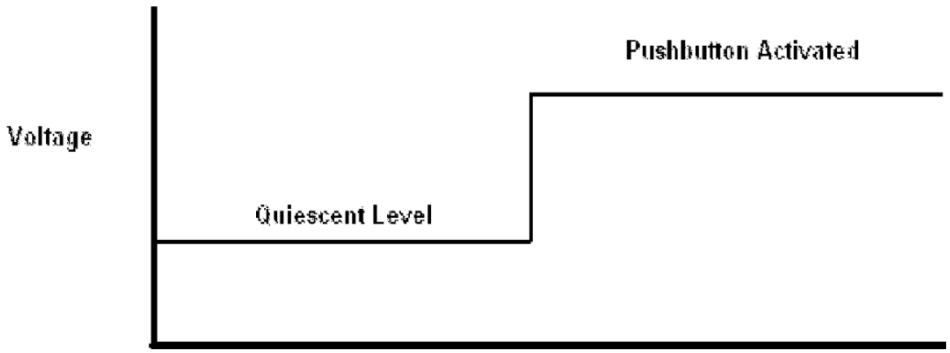


Figure 2: Simplified diagram of Bovie Electrosurgical Generator output waveform, clearly identifying a lower quiescent voltage when the device is off.

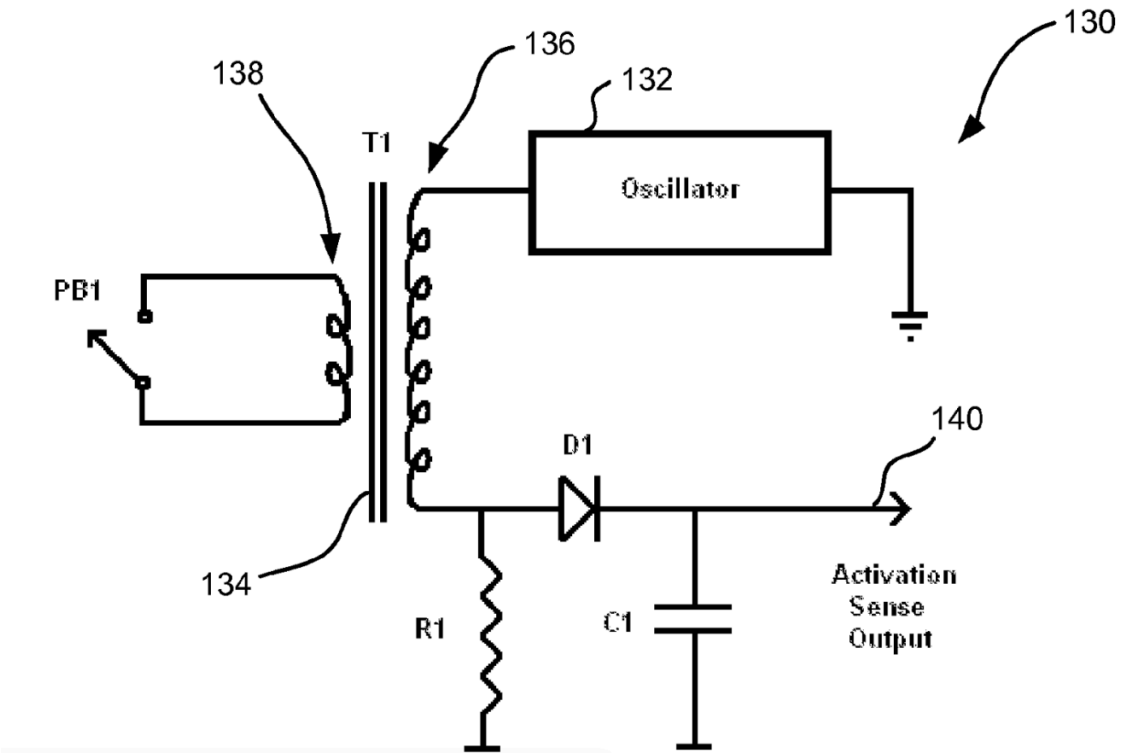


Figure 3: Simplified output diagram of Bovie Electrosurgical Unit

2.1.2 Mid Voltage

The mid voltage stage is responsible for taking high voltage AC input (80V-100V) at high frequencies of 50kHz to 100kHz, and stepping this down to a 5V DC output, within acceptable ripple tolerances. This is achieved via a full bridge rectifier using four 200V 400mA fast recovery shotkey diodes and a 100µF 160V output filter capacitor. This is then fed into the heart of the system, an LM5168 120V wide input voltage synchronous buck converter. This steps the input voltage down to 5V, and provides the line and load regulation for the output. The Schematic and PCB layout are given in appendix B.

The Mid Voltage stage has a few key subsystems that ensure correct operation. The Full bridge rectifier composed of diodes D1,D2,D3,D4, and input screw terminal J1 connect to the input from a stepped down waveform from the ESU (nominally 100V AC, 50kHz - 100kHz). This stage converts the input into pulsed DC. The capacitor bank composed of CFB, CIN1, CIN2, CFILT3, and CFILT 4 serves a variety of functions for the device. CFB is a large capacitor that is designed to smooth the pulsed AC into low ripple DC. CIN1 and CIN2 provide charge storage for the pulsed current demands of the buck converter. CFILT3 and CFILT4 are 10nF each, and provide a low impedance path for high frequency noise,

to prevent it from propagating through the device and disrupting operation. At the heart of the design is the LM5168 buck converter (U1). The output filters of L and C were calculated using these formulas [3].

$$L = \frac{(V_{in} - V_{out})}{K \cdot I_{out} \cdot F_{SW}} \cdot \frac{V_{out}}{V_{in}} \quad (2.1)$$

$$C > \frac{\Delta i_L}{8 \cdot F_{SW} \cdot \Delta v_O} \quad (2.2)$$

$$\Delta i_L = \frac{V_{in}}{L \cdot F_{SW}} \cdot \frac{V_{out}}{V_{in}} \quad (2.3)$$

Where, K is the desired ripple factor, which was selected to be 0.2 to minimize inductor current ripple, and thus output voltage ripple.The output voltage ripple, Δv_O, was desired to be less than 5% of output, which limits output voltage ripple to 250mV. From these equations, the inductor value was chosen to be 120µH, and the output filtering capacitor COUT1 was chosen to be 22µF, which is a standard package size. Additionally CFILT1 and CFILT2, both 10nF, were added to the output to further filter high frequency noise. The switching frequency of the converter was a critical decision, as this would determine the sizing of the output inductor and capacitor. As the duty cycle on this converter is very low, the switching frequency may not be too fast as to be limited by the MOSFET turn on and turn off time. At the same time, a slow switching frequency requires larger Inductors and capacitors to achieve the same output ripple, thus increasing the boards size, and component cost. Per recommendations in the datasheet, the switching frequency was set to 750 kHz. Other components, such as feedback resistors and enable resistors were sized appropriately using relatively trivial equations found in the LM5168 datasheet [3].

On the PCB, a few key design decisions are important to note. Due to the high current transients present in the buck converter, all traces supplying power to and from the buck converter are needed to be kept as short as possible. Additionally, the high frequency filtering capacitors must be placed as close as possible to the input and outputs of the devices, seen with CFILT3 and CFILT4 being extremely close to the Vin pad of the LM5168. Again this is to reduce the parasitic inductances created by the PCB traces. Additionally, the switch node pad is incredibly noisy, due to the switching nature of buck converters, and must be a reasonable distance away from the feedback line to ensure safe operation. To add additional shielding to the feedback line, a ground pad has been strategically placed in between the switch node and feedback trace. Vias have been placed around the buck converter to aid with thermal dissipation and noise shielding. All power traces have been increased to 40 mil,to decrease DC resistance and provide better thermal performance. Much of the PCB criteria was guided by IPC-2221A criteria [4] After performing well in simulation, as seen in Figure 4, this design was released to manufacturing.

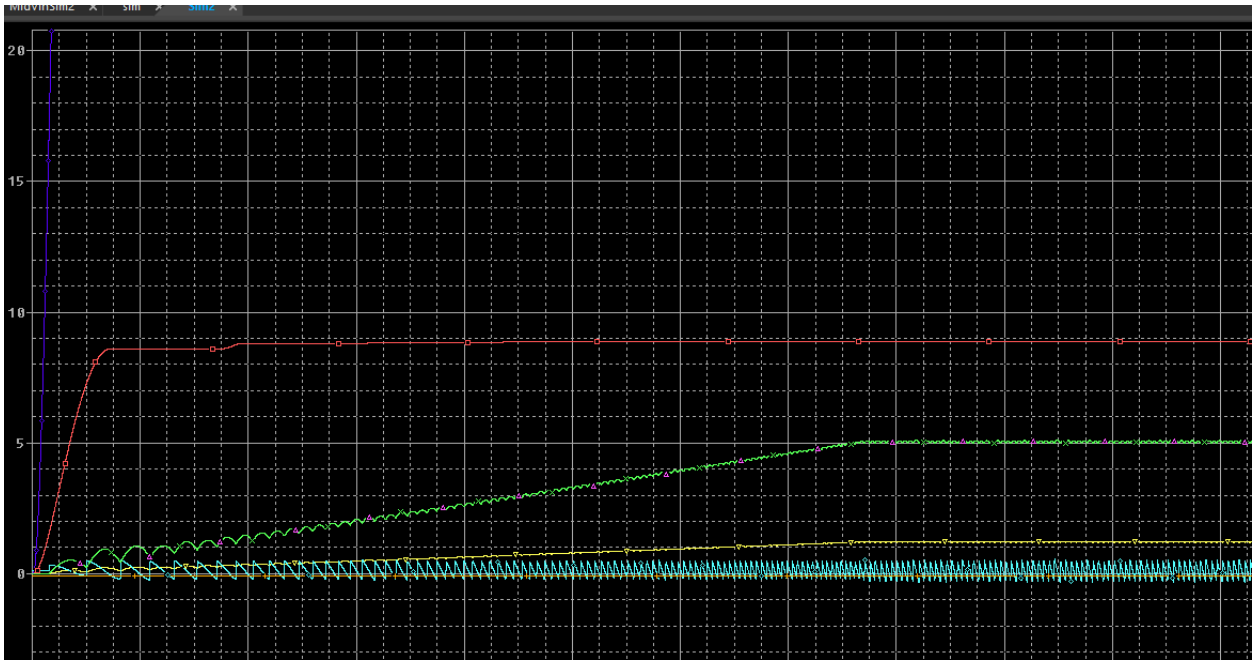


Figure 4: PSpice simulation of Mid Voltage stage, confirming behavior. Traces are as follows: Blue, V_{In} Red, Enable, Green, V_{Out}, Yellow, Feedback, and Cyan, Inductor current

2.2 Low Voltage Signal Processing and Waveform Generation

2.2.1 Cautery Tool Monitor

To create the cautery tool monitor, carrier AC source generates a high-frequency sine wave at a 925 V amplitude and 925 DC offset, with the frequency set to 307 kHz. This directly matches the specifications in the BOVIE cautery manual **[2]** the medical team had us use as reference. This design was tested with an ON cycle of 1 ms and OFF for 4 ms, and an ON cycle of 19 µs and OFF for 19 µs using a wave generator to simulate the BOVIE source repetition documentation. Components C1 (10 pF), and C2 (3.9 nF) are used to create the capacitance voltage divider. This is because at high frequencies, like the 307 kHz, capacitors have an impedance, and they divide AC voltage just like resistors divide DC voltage. A 10 kΩ resistor is also used to provide a DC path to ground so the output signal is not "floating". Also, this resistor is large enough to have no impact on the AC signal division, as 133 Ω is much less than the 10 kΩ . The voltage divider with the 2000 V AC source is shown in Figure 5.

$$Capacitive\ Resistance\text{: } Xc = \frac{1}{2*\pi*f*C} = \frac{1}{2*\pi*307{,}000*3.9*10^{-9}} = 133\ \Omega \qquad (2.3)$$

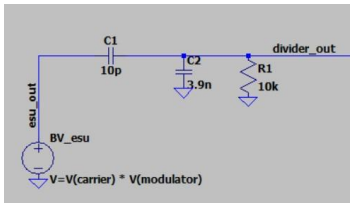


Figure 5: 2000V AC Source Capacitance Voltage Divider

$$Ratio = \frac{10pF}{10pF+3900pF} = \frac{10}{3910} = \frac{1}{391} \quad (2.4)$$

$$Peak\ Voltage\ Reduction: 1850V * Ratio = 1850 \div 391 = 4.7\,V \quad (2.5)$$

A 2.2 nF capacitor is used when the input signal is much lower in voltage, and because of the same high frequency signal used, has the exact same output as the capacitance voltage divider above. This design is shown in Figure 6.

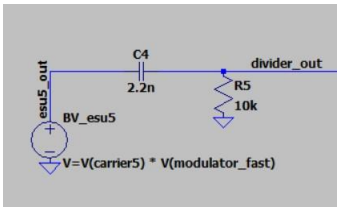


Figure 6: 5-20V AC Source

The next step is envelope detection which is used to output detect when the AC signal is ON vs OFF. This is fed into a comparator to output 5V when the AC signal is ON and 0V when the AC signal is OFF. The components used for this part are D1 (1N5817), R2 (5.6 kΩ), and C3 (1 nF). The diode D1 acts as a half-wave rectifier, allowing current to pass only on the positive peaks of the signal, which charges capacitor C3. When the carrier signal stops, D1 stops conducting, and C3 slowly discharges through R2. The result at the envelope node is a DC-like voltage that rises when the signal is present and falls when it's absent.

$$\frac{1}{307kHz} \approx 3.26\mu s \quad (2.6)$$

$$\tau = R * C = 5,600\,\Omega * 0.001\,\mu F = 5.6\,\mu s \quad (2.7)$$

The 5.6 µs time constant is long enough that C3 doesn't discharge too much between the 307 kHz peaks, preventing excessive ripple. Also, 5.6 µs must be shorter than the "off" time, where it is for both the 19 µs and 2 ms OFF cycles signals. The 1N5817 is a Schottky diode, It is used for its low forward voltage drop (so it can efficiently rectify even small signals) and its fast switching speed, which is necessary to handle the 307 kHz frequency.

The other components used in this part are U1 (LM393A), R6 (47kΩ), R3 (3kΩ), R4 (10kΩ). The comparator U1 (LM393A), compares the envelope voltage (on its positive input) to a fixed reference voltage (on its negative input). If $V_{envelope} > V_{reference}$, the output goes HIGH. If $V_{envelope} < V_{reference}$, the output goes LOW. The envelope detector and comparator is shown in Figure 7.

$$V_{reference} = 5V * (\frac{R3}{R6+R3}) \approx 0.3V \quad (2.8)$$

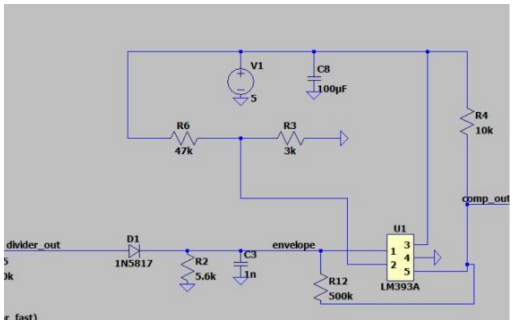


Figure 7: Envelope Detector & Comparator

This 0.3 V threshold is low enough to be reliably triggered by the envelope detector but high enough to ignore any small noise when the signal is off. The LM393 has an "open-collector" output, meaning it can only pull the output down to ground. R4 is used as a pull-up resistor for the comparator. When the comparator's output is "high" (inactive), this resistor pulls the comp_out voltage up to the 3.3 V supply rail as needed. 10 kΩ is a standard value that works well in most (including this) digital logic applications.

The entire design for the ESU Monitor circuit is shown below in Figure 8.

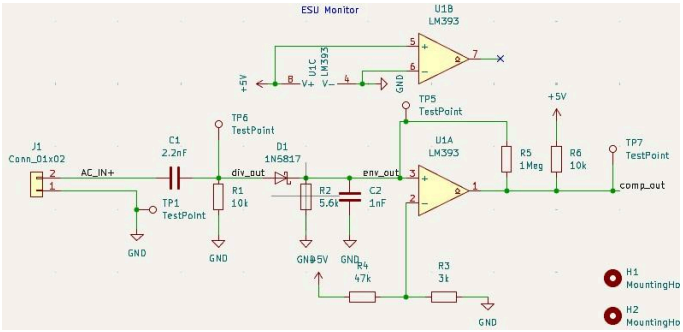


Figure 8: ESU Monitor Circuit

2.2.2 Microcontroller

The ATtiny85 microcontroller is used with a programmer to detect the Duty cycle of the AC signal and output 5 V on the off portions of the signal. Comp_out, the output of the cautery tool monitor, feeds into pin3 and the output on pin4. The schematic of the microcontroller portion of the design is in Figure 9.

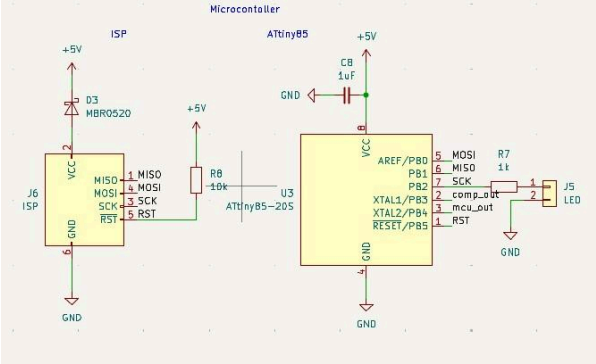


Figure 9: Microcontroller Schematic

2.2.3 Pulse Generator

The entire nerve stimulation output needs to be **50 Hz - 1 kHz with a Pulse width of 100 µs - 1 ms at 0.1 V [3],** whose specifications were given by the medical team**.** In order to generate a pulse that fits the frequency and pulse width requirements, a N555 timer is used. With the discharge transistor off, the timing capacitor, C9 (0.01 µF), begins to charge through the timing resistors, R9 (15 kΩ) and R10 (130 kΩ). A diode is also used to time high, where it acts as an open circuit, and time low, where it acts as a closed circuit. Both of these formulas are calculated below. The duration of the output pulse is determined by the time it takes for the voltage across C9 to reach two-thirds of the supply voltage. This voltage is monitored by the timer's threshold pin (pin 6).

$$T_{high} = 0.693 \cdot R_a \cdot C = 0.693 \cdot 15{,}000\ \Omega \cdot 10^{-8}\ F = 1.04 \times 10^{-4}\ s = 100\ \mu s \quad (2.9)$$

$$T_{low} = 0.693 \cdot R_b \cdot C = 0.693 \cdot 130{,}000\ \Omega \cdot 10^{-8}\ F = 9.01 \times 10^{-4}\ s = 900\ \mu s \quad (2.10)$$

This creates a pulse signal of 1 kHz with a pulse width of 100 µs, which is what we need from the medical team specifications. The output voltage is 3.3-3.5 V when high, as there is a voltage drop of 1.5-1.7 V caused by the timer's internal circuitry. The circuit diagram of the pulse generator is shown below in Figure 10.

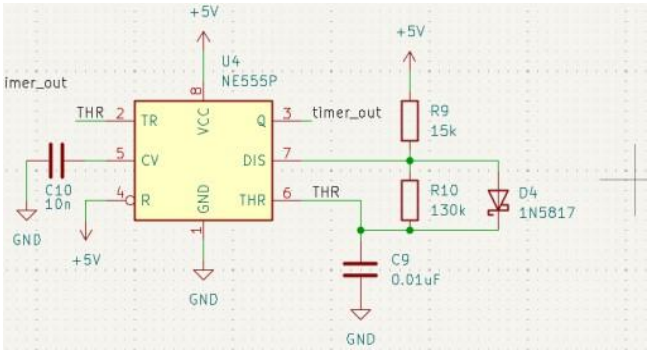


Figure 10: Timer Circuit Schematic

2.2.4 Neurostimulation Output

For the neurostimulation output, the Mosfet acts as the gate, where the mcu_out is the gate driver and the pulse as the source. This outputs the nerve stimulation waveform when both the mcu_out and pulse signal is high. This creates a 5 V DC signal of 1 kHz with a pulse width of 100 µs. However this signal has a lot of noise, which needs to be scrubbed away.

The last portion of the circuit designed is the output. This uses a LM393 comparator with the reference voltage of 1 V (through a voltage divider of 5 kΩ and 1 kΩ), and the positive being the drain of the mosfet above, which when high is 3.3-3.5 V, higher than the 1 V reference as needed. A diode is also used to prevent noise in the output from the mosfet (acts as an open circuit in the direction from drain to gnd). This outputs a steady, noise free 5 V when input is above 1 V, which the drain of the mosfet will be when both the mcu_out and pulse signal is high. Lastly a voltage divider is used to output a 0.1 V signal of 520 Hz with a pulse width of 1 ms, which is well within the specifications of the neurostimulation output.

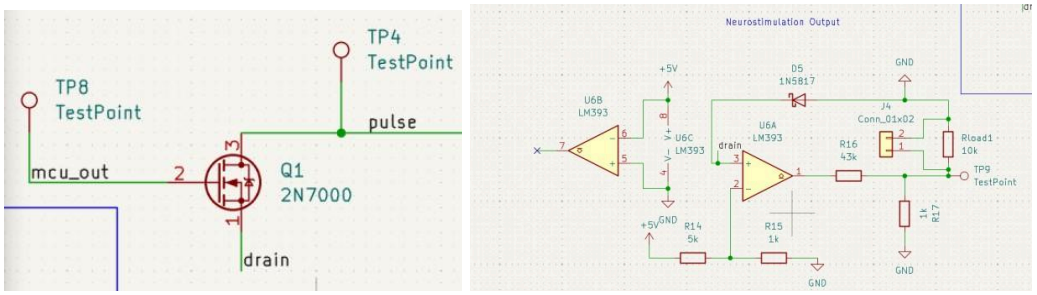


Figure 11 & 12: Mosfet & Neurostimulation Output Comparator Circuit Schematic

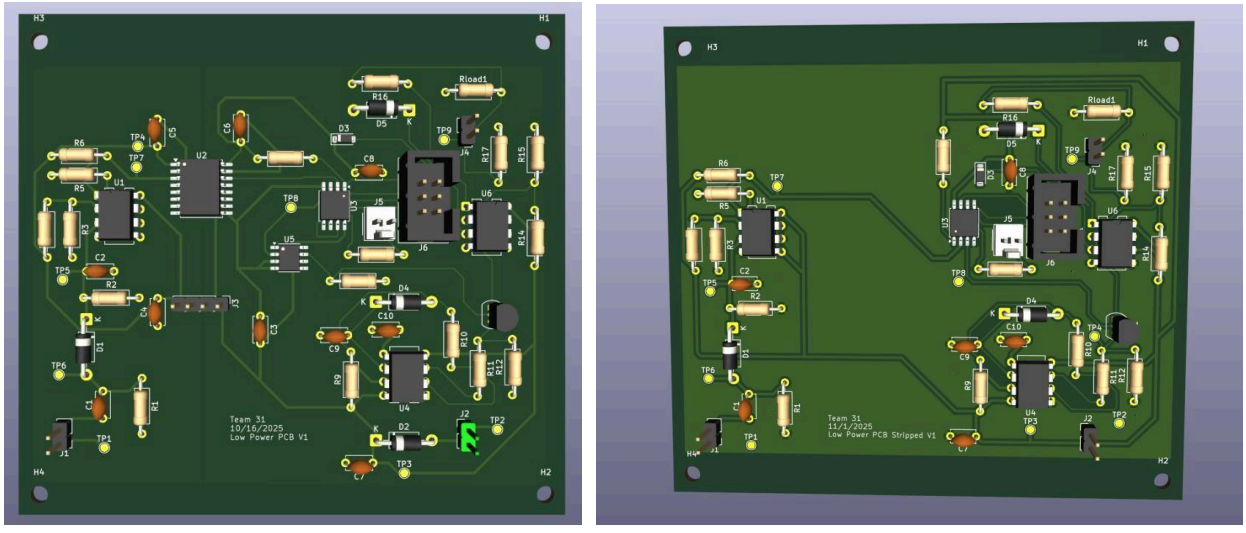


Figure 13 & 14: 3D rendering of Low Power PCB with Voltage Isolation & Low Power PCB without Voltage Isolation

3. Design Verification

3.1 Verification of Neurostimulatory waveforms and ESU Monitor

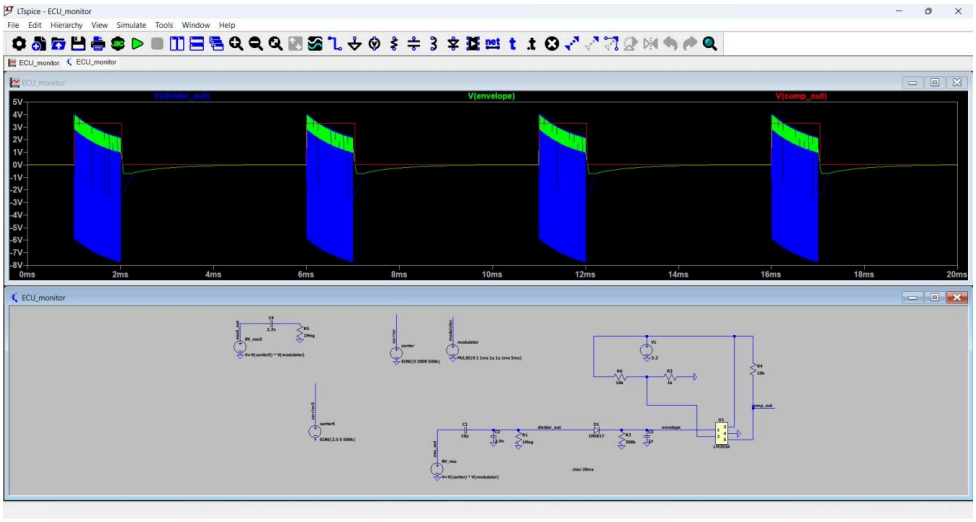


Figure 15: Envelope Detection and Comparator Simulation

Envelope Detection and comparator simulation verification in Figure 15, which shows the circuit accurately detects when the AC source is ON and output 5 V.

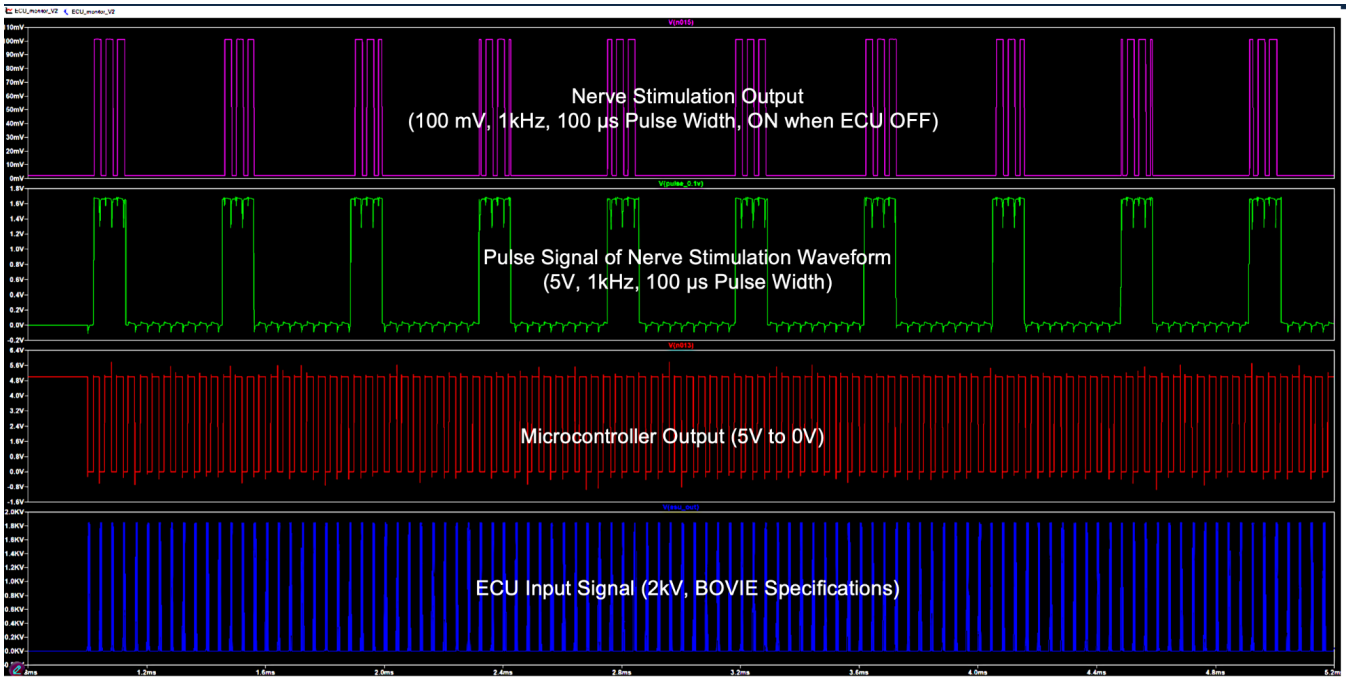
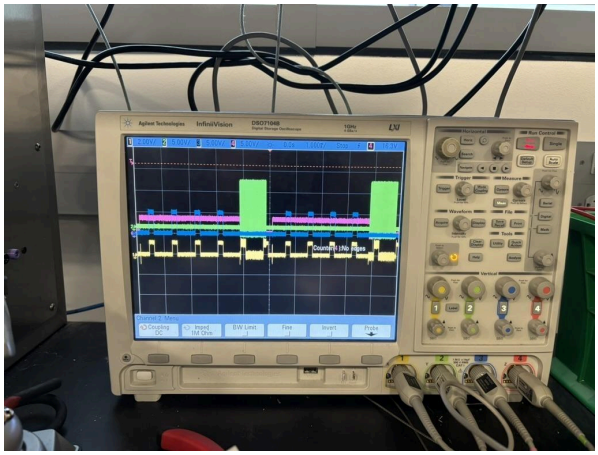


Figure 16: Neurostimulation Waveform Output Bovie Specifications

In Figure 16, nerve stimulation pulse output (green) works when outputting with BOVIE specifications (with about a 4 µs delay), which is expected.

Figure 17: Completed nerve stimulatory waveform generation PCB



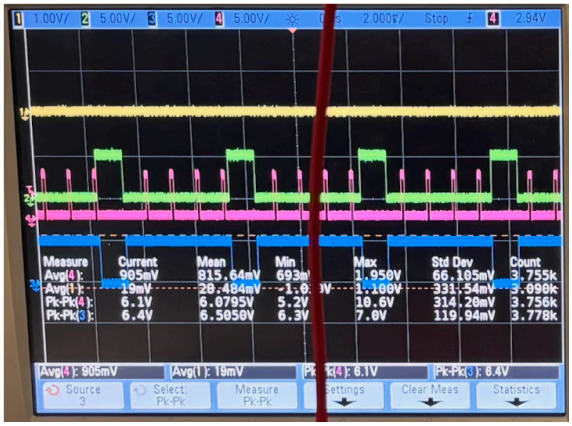


Figure 18 & 19: Final PCB Output

The Figure 16 oscilloscope the output of the microcontroller (pink left, blue right) accurately detects when the AC signal (green) is ON. This breadboard design of the circuit above also shows the output pulse signal(blue left, pink right) is within what the specs should be, and the mosfet/comparator is accurately working to only output high (5V) when both the microcontroller output and pulse signal is high, which it is. All voltages are within the 0.5V tolerance described in the design report.

3.2 Verification of Mid Voltage Stage

After being constructed, the Mid Voltage stage was verified through oscilloscope measurements of the output, of both the 5V DC output and rectified AC input to the buck converter. A variac providing variable 60Hz AC sine wave was used as the input to the device. The results are as follows.

Table 1: Verification of Mid Voltage Stage

Load	Output Voltage	Output Ripple	AC Input	Rectified DC	Rectified DC Ripple
100mA	5V	288 mV	40V	39.6V	6.9V
0mA	5V	1400mV	40V	39.6V	6.9V

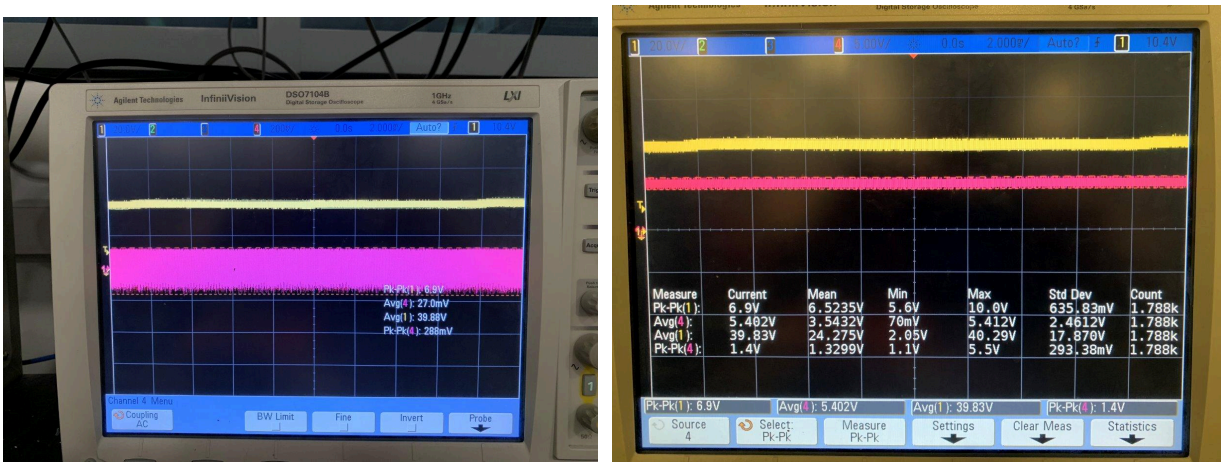


Figure 20 & 21: Oscilloscope Measurements of Mid Voltage Stage with No Load (right) and Full Load (100mA, left)

4. Costs

4.1 Parts

Table 2: Parts Costs For Mid Voltage Stage

Part Number	Manufacturer	Retail Cost ($)	Bulk Purchase Cost (1k units) ($)	Actual Cost ($)
BAV21W-7-F	Diodes Incorporated	0.10	0.039	0.40
OSTTC022162	On Shore Technology	0.57	0.2248	1.14
EKMQ16ELL101MK25S	Chemi-Con	1.14	0.3725	1.13
C201X5R2A475K125AC	TDK Corporation	0.75	0.2529	1.5
C06003C103K2RECTU	KEMET	0.15	0.03633	0.3
RC0603FR-07100KL	YAGEO	0.1	0.0052	0.1
RC0603JR-070RL	YAGEO	0.1	0.00384	0.1
RLB0712-121KL	Bourns Inc.	0.28	0.158	0.28
C0603C222J2GACTU	KEMET	0.11	0.02416	0.11
CRCW060333K2FKEAC	Vishay Dale	0.1	0.008	0.1
CL32A226KAJNNNE	Samsung Electro-Mechanics	0.47	0.143	0.47
C0603C103K5RACTU	KEMET	0.08	0.009	0.08
RC0603FR-07196KL	YAGEO	0.1	0.0052	0.1
CR0603-FX06192ELF	Bourns Inc.	0.1	0.0048	0.1
CMF5550R000FKEK70	Vishay Dale	0.56	0.173	0.56
LM5168FDDAR	Texas Instruments	2.09	1.1058	2.09
Total	-	-	**2.5663**	**8.56**

Table 3: Part Costs for Low Voltage Stage

Part Number	Manufacturer	Description	Quantity	Retail Cost (USD) $	Bulk Purchase Cost (1k Units) ($)	Actual Cost ($)
296-6501-2-ND	Texas Instruments	IC OSC SGL TIMER 100KHZ 8-SOIC	1	0.28	0.12315	0.28
TC4426ACPA	Microchip Technology	IC GATE DRVR LOW-SIDE 8DIP	1	1.54	1.17	1.54
CPF0805B49K9E	TE Connectivity	49 kΩ, 0.1% resistor, 0603	1	0.11	0.11	0.11

	Passive Product					
RT0402BRD0715KL	YAGEO	15 kOhms 0.1% resistor, 0.063W	1	0.17	0.04567	0.17
RG2012P-102-B-T5	Susumu	1 kΩ, 0.1% resistor, 0603	1	0.1	0.04774	0.1
ERA-2AEB103X	Panasonic Electronic Components	10 kΩ, 0.1% resistor, 0603	3	0.1	0.05637	0.3
CC0402KRX7R9BB103	YAGEO	0.1µF, 50 V, 0402	2	0.08	0.0032	0.16
1N5817	SMC Diode Solutions	DIODE SCHOTTKY 20V 1A	2	0.18	0.04412	0.36
DMPH16M1UPSW-13	Diodes Incorporated	12V N-MOS 12-V, Surface Mount	1	0.32	0.32	0.32
0603N100J500CT	Walsin Technology Corporation	10 pF, 50V Ceramic Capacitor, 0603	1	0.1	0.00824	0.1
GRM155R71H392JA01D	Murata Electronics	3.9 nF, 50V Ceramic Capacitor, 0603	1	0.1	0.01043	0.1
CL21B102KBANNNC	Samsung Electro-Mechanics	1 nF, 50V, Ceramic Capacitor, 0805	1	0.1	0.01176	0.1
RMCF0603FT3K00	Stackpole Electronics	3 kΩ, 1% resistor, 0603	1	0.1	0.0048	0.1
RMCF0603FT5K60	Stackpole Electronics	5.6 kΩ, 1% resistor, 0603	1	0.1	0.0048	0.1
RMCF0603FT47K0	Stackpole Electronics	47 kΩ, 1% resistor, 0603	1	0.1	0.0048	0.1
LM393ADR	Texas Instruments	Comparator (General Purpose) Open-Collector	1	0.37	0.16465	0.37
ATTINY85-20SU	Microchip Technology	IC MCU 8BIT 8KB FLASH 8SOIC	2	1.50	1.25	3.00
Total				5.35	3.38	7.31

4.2 Labor

Table 4: Labor Costs

Team Member	$/hr	Total Hours	Cost (USD) $
Stephen	$40*2.5	10 hrs per week for 14 weeks	$14,000
Aidan	$40*2.5	10 hrs per week for 14 weeks	$14,000
Alex	$40*2.5	10 hrs per week for 14 weeks	$14,000
Total			$42,000

5. Conclusion

5.1 Accomplishments

Our design met all requirements the medical team of Neuroguard had us design. Our design worked both in simulation, and under ECE 445 lab constraints, worked as well. Our team persisted in the phase of PCB delays, difficulty with high voltage testing, and technical difficulties in the construct

5.2 Uncertainties

2kV testing was unable to be done in ECE 445 lab. Because of this, we are unsure if our high voltage design proposal is suitable for implementation with the Bovie ESU. There are concerts that as the device is triggered by output impedance, connecting a power supply to the output, which is needed to power the Neuroguard, may hinder operation, or inadvertently draw too much current and cause

5.3 Ethical considerations

With any device implemented in a medical setting, strict ethical considerations must be in place to ensure that no harm is done to the patient. This includes rigorous testing of the device, to ensure that to the fullest extent of our knowledge that it can work as prescribed, without causing harm to the patient. As a higher bar than doing no harm, we must demonstrate substantial beneficence to the patient, to ensure the device is not used needlessly.

5.4 Future work

While our work this semester in ECE445 has been fruitful in creating useful hardware for the neuroguard team, there is still much work to be done. The first course of action we recommend is a full characterization of the output of the Bovie Electrosurgical Generator. This will allow us to then design

the proper hardware interface for the waveforms that are created. Without knowing the output forms of the ESG, we cannot successfully design any interface for the device. The next step would be to research and model the nerve stimulation and activation. This will involve creating finite element models of the tissue around the nerve during surgery, and the behavior of the ICBN itself, in order to tune the somatosensory evoked potentials. Then signal processing algorithms must be designed to convert electrode information of the evoked nerve into numerical approximations for distance the cautery pen is to the nerve. All of this must be followed by rigorous testing to ensure the device behaves properly and reliably before applications can be submitted to the appropriate government agency for regulatory approval, and eventual commercial release. This is a long and difficult road, littered with technical challenges and pitfalls, but we are confident that with the start we have made in ECE 445, the neuroguard team will be sure to succeed.

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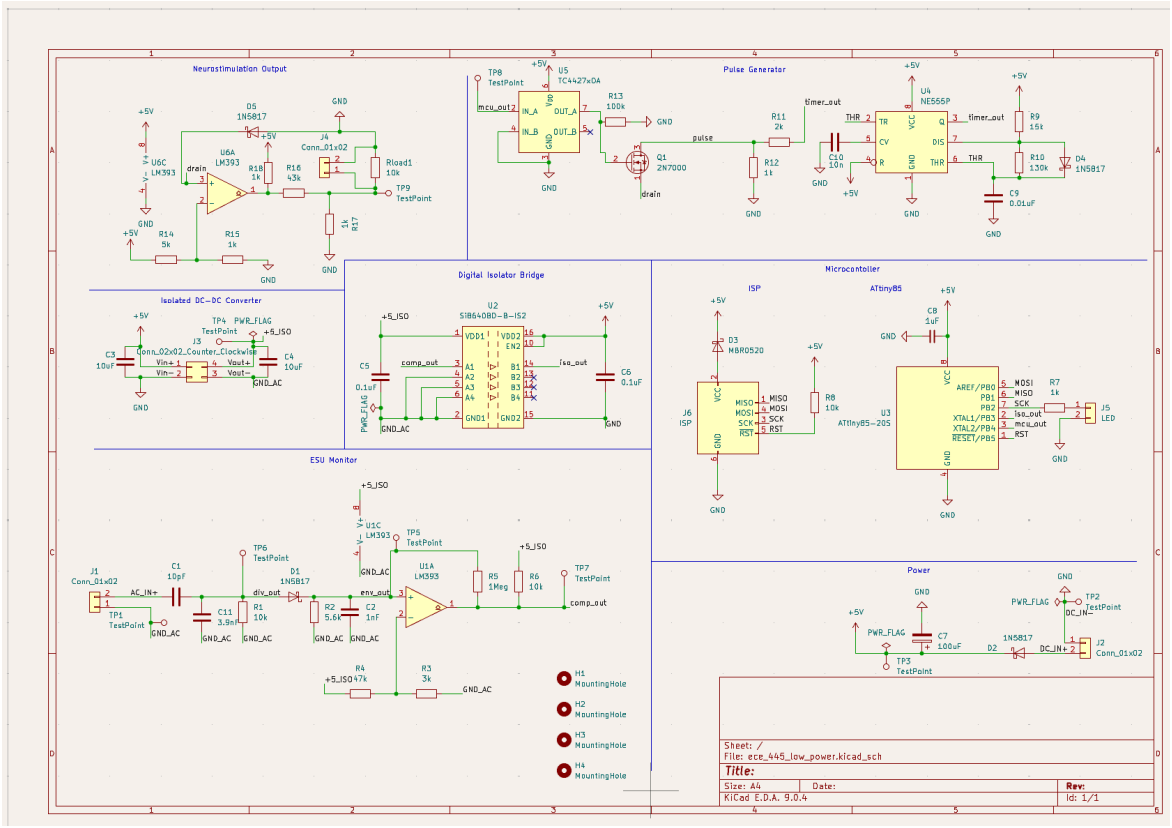
Appendix A Requirement and Verification Table

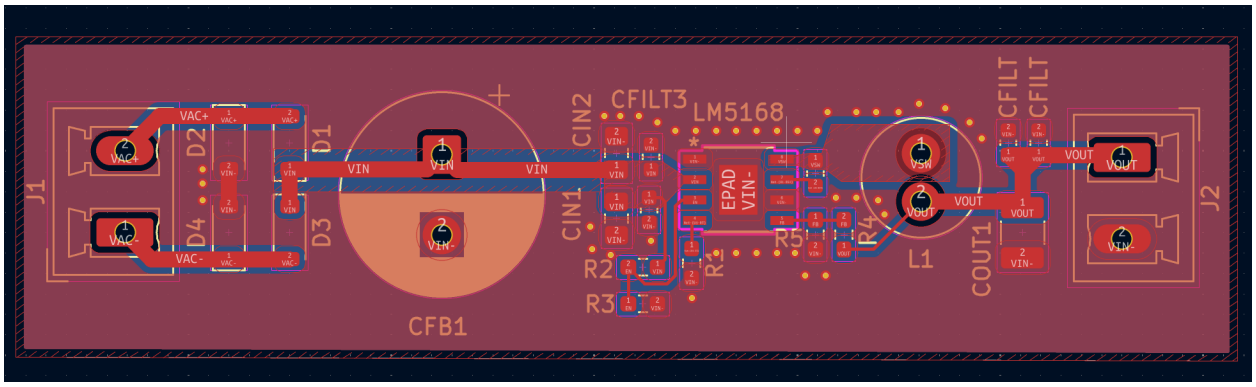
System Requirements and Verifications

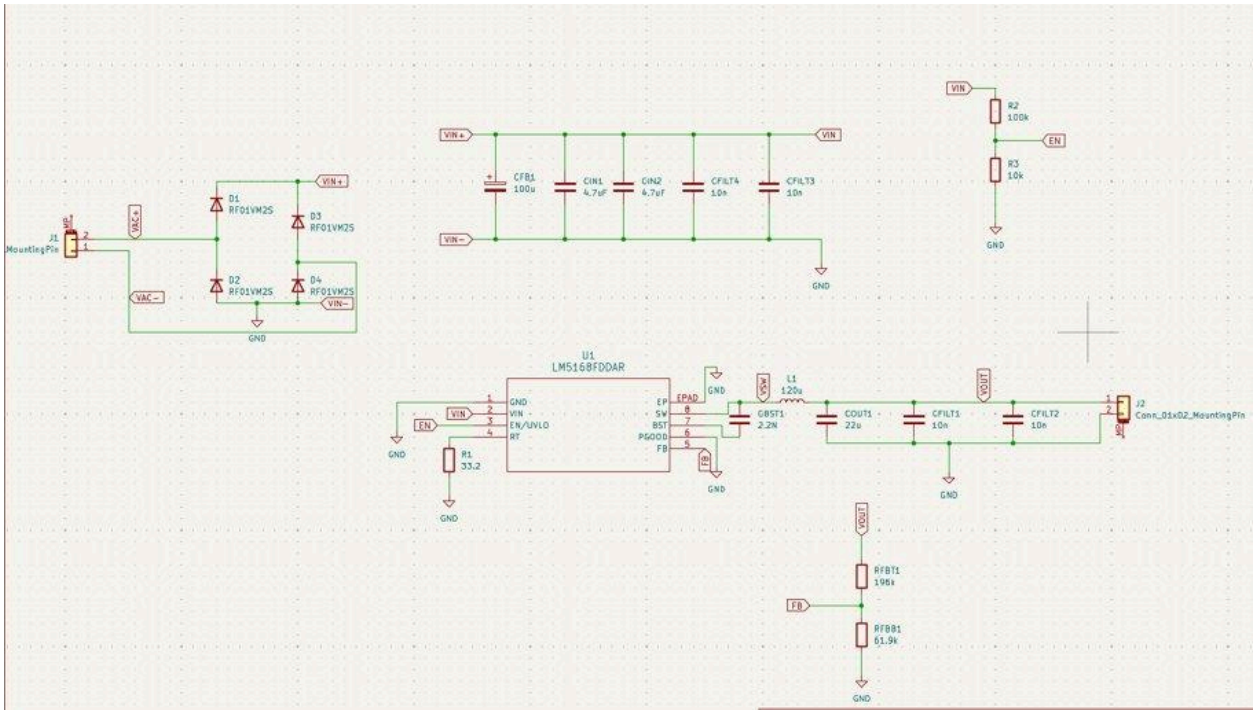
Requirement	Verification	Verification status (Y or N)
Buck converter outputs 5V at 100mA, output voltage ripple is less than 0.25V	Oscilloscope measurement of output voltage with resistive load of 50Ω. Input power will be from Variac. Input will start at 30V AC and increment to 100V AC once safe device behavior is confirmed.	Y
Full bridge rectifier archives output DC voltage of 100V with voltage ripple less than 2V	Oscilloscope measurement of Vin trace	Y
Buck converter can handle 100mA to 300mA output transient in <10 uS.	Oscilloscope measurement of Vout with electronic load.	Did not have suitable E-Load to rigorously test this
3. The signal at pulse is measured to be 5V, outputting at the frequency desired between 50Hz-1kHz, and a pulse width between 100us - 1ms.	• Probe test divider_out using a multimeter • Confirm multimeter matches simulation waveform/breadboard results and is measured between the requirements listed.	Y
4. Confirm output is only high when microcontroller_out is high	• Probe inputs and outputs of comparator with multimeter. • Confirm Vref is input voltage is correct	Y
5. The V(divider_out) positive peak is greater than 0.5V, which is more than the 0.3V threshold needed by the comparator.	• Probe test divider_out using a multimeter • Confirm multimeter matches simulation waveform/breadboard results and is measured between the requirements listed.	Y
6. The Vref of the comparator is measured to be 0.3V with 5% tolerance. The output of the comparator is measured to be 3.3V when the input envelope detector is above 0.3V and 0V when below.	• Probe inputs and outputs of comparator with multimeter. • Confirm Vref is input voltage is correct	Y
7. When input voltage to microcontroller_in is LOW, then microcontroller_out is 5V.	• Probe input and output of microcontroller with multimeter.	Y

Appendix B Full PCB Schematics



PCB Layout of Mid Voltage Stage





Full Schematic of Mid Voltage Stage