SOUND ASLEEP

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Abstract

This project implements a closed-loop sleep enhancement system that delivers pink-noise stimulation during slow-wave sleep (SWS). The system consists of a wearable EEG electrode headband connected to the ADS1299 ADC and STM32WB5 microcontroller which converts and streams 8 channels of EEG data over Bluetooth Low Energy (BLE). A mobile application decodes the data in real time, visualizes the EEG, and controls stimulation parameters using either a classical YASA-based detector or an adaptive CoSleep algorithm. The app also provides calibration tools, safety-limited volume control, and detailed event logging.

Project testing verified reliable BLE streaming at 50 Hz, stable multi-channel visualization, and audio stimulation latency near 120ms, consistent with published requirements for SWS enhancement. The results demonstrate a functional prototype capable of real-time monitoring and closed-loop auditory stimulation intended to improve slow-wave sleep depth.

Contents

1. Introduction

This section highlights the common issues of a lower amplitude and smaller longevity of slow wave sleep in need of a solution. Our project, Sound Asleep, offers a solution to this problem.

1.1 The Problem

Slow-wave sleep (SWS) is critical for memory consolidation, immune function, and overall health, yet many people experience insufficient or low-quality SWS. Most commercial sleep trackers only monitor sleep and do not intervene to improve it, while EEG-based devices are often uncomfortable for overnight use or lack real-time stimulation capabilities. Research in auditory closed-loop stimulation shows that precisely timed pink-noise pulses can strengthen slow waves and enhance sleep quality, but current solutions are bulky, proprietary, or inaccessible to typical users.

1.2 The Solution

Sound Asleep provides a comfortable, wireless, and fully real-time system to detect and enhance SWS. A lightweight EEG headband records brain activity and streams it via Bluetooth to a mobile application. The app analyzes EEG signals, identifies slow-wave activity, and triggers pink-noise bursts through the user's own audio device at precise phases of the sleep cycle. By combining accurate EEG sensing with closed-loop stimulation in a user-friendly form, Sound Asleep transforms laboratory techniques into a practical, consumer-ready sleep enhancement tool.

1.3 System Block Design

The system block diagram shown in Figure 1 is divided into 3 key sections. The first is the EEG Headband which outputs EEG readings at a maximum magnitude of 50 uV to the transmission board. The transmission board receives that data and filters it in preparation for the analog to digital converter. The analog to digital converter will send a packet via SPI to the microcontroller in preparation for a BLE packet transmission. The transmission board is also designed with the appropriate power system that also allows for a 9V rechargeable battery to be recharged. The 16 byte packet of EEG is transmitted to a mobile app via BLE. The app then receives the data, processes the data using ML algorithms, and triggers a pink noise stimulation based on slow wave sleep activity.

The block diagram originally consisted of a 21 electrode input which is a much larger input than what is necessary for slow wave sleep detection. This was revised to an 8 electrode headband which is much more comfortable and does not require excess pin inputs. Filtering was also added to reduce the noise on the electrodes which is a significant factor due to the extremely low magnitude of EEG signals. The ADC was also not in the original design since we had thought the MCU could handle the ADC which was not possible once entering the hardware development stage. This is also due to the low magnitude of the signals which require a higher precision and amplification which the ADS1299 offers. The rechargeable design was also added as a way to allow the user to not have to replace the battery after each use due to the high power consumption of the device.

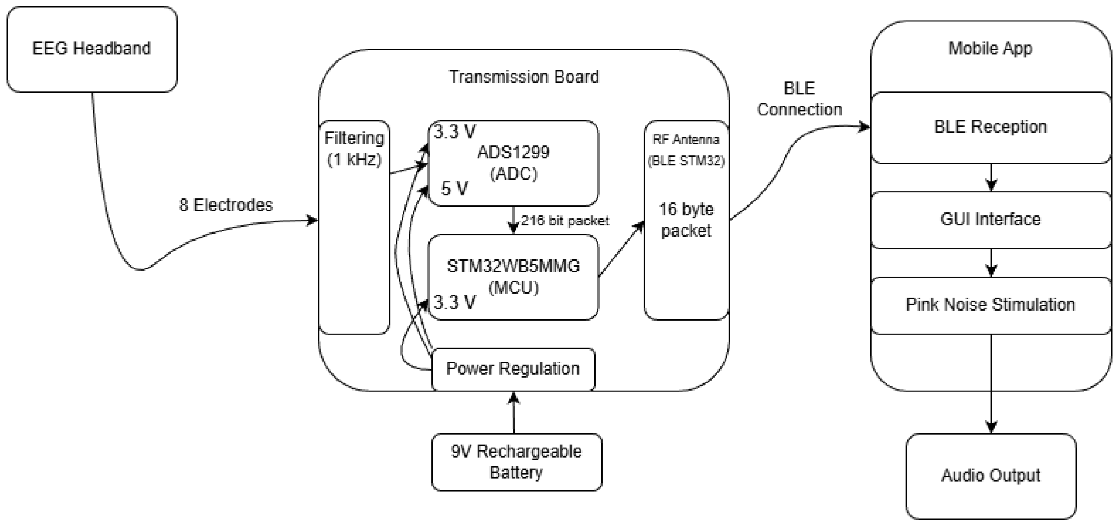

Figure 1: Final Design Block Diagram

2. Design

The design for Sound Asleep was split into hardware design(selecting the appropriate hardware components), schematic/pcb design(placing our selected components), firmware design (for BLE functionality of PCB as a transmitter) and application design (for BLE as a receiver, connectivity to user audio device and analysis of EEG signal data) as shown in our block diagram.

2.1 Hardware Design

The hardware design involved selecting components for our overall transmission board and understanding the EEG subsystem for proper data collection/transmission.

2.1.1 Microcontroller

The microcontroller that was chosen for the design is the STM32WB5MMG MCU shown in Figure 2. This microcontroller is built off of the STM32WB55, but has some RF components built into the package. This specific package was chosen due to its BLE capabilities and the accessibility of built in RF components. The available High Speed External Oscillator (HSE) and Low Speed External Oscillator (LSE) along with an antenna on the device allow for full focus on the digital aspect of using BLE. The STM32WB5MMG has many powering modes for the device. We had thought originally that one could simply use the VBAT pin in order to power the device without needing to use both an analog and digital supply. That is correct, however, the entire chip will not be powered. Only certain components like the real-time clock (RTC) and back up registers will be powered in order to keep the device ready for its next use when it is powered. The board had to be revised in order to fix this mistake. This issue had also occurred because the schematic component had mislabeled VDD as VDDSMPS, so I had thought there was no VDD pin. This MCU has many pins ready for simple GPIO and SPI configuration which were used for the firmware with the analog to digital converter.

Figure 2: STM32WB5MMG Microcontroller Package

2.1.2 Analog-to-Digital Converter

The ADS1299 is an 8-channel, 24-bit analog to digital converter (ADC) that specializes in EEG data. This IC is crucial to the design of the PCB because it sends the EEG data to the MCU for processing/transmission. The ADS1299 requires a digital and analog power supply. The digital power supply can be a common 3.3V rail that can be shared with the MCU. The analog power supply has multiple options that can be used to power it. For the current design, we chose to use the unipolar 5V input to reduce complexity, but using a 2.5V and -2.5V bipolar supply in the future would allow us to reduce the size of the battery to a 3.7V battery instead of 9V. We planned to make this design choice with an updated design of the PCB which would require an updated power system.

There was a common application in the datasheet for this chip which was used as reference for the design. They had no recommendations for picking the resistance and capacitance for the filtering on the electrodes so we made an estimate of 100k ohm resistance and 1.5 nF capacitance to give a roughly 1 kHz cutoff since we didn't want to filter frequencies that would be within our EEG range. This was calculated using the following equation where R is the resistance and C is the capacitance.

$$f_c = \frac{1}{2\pi RC} = 1060\ Hz = \frac{1}{2\pi(100*10^3\ \Omega)(1.5*10^{-9}\ F)} \quad (1)$$

This cutoff frequency was decided based on an upper limit in EEG data frequencies at 500-2000 Hz which is not necessary for our device. In hindsight, we believe that this frequency could be lowered to a 100 Hz range as medical EEGs usually only receive high gamma values at 80 Hz for proper medical brain wave readings.

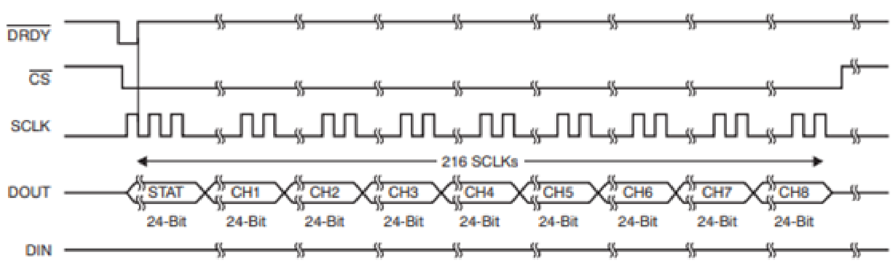

Figure 3: SPI Bus Data Output

This system will communicate with our microcontroller with 2 different methods. The first method is 4 common GPIO pins which allow the microcontroller to set up registers or activate settings on the ADS1299. We chose to attach those to common GPIO pins on the MCU that were not being used by anything else and were easily routable in the PCB design. The other, and more important, method that this device uses to communicate is through a serial peripheral interface (SPI). This method connects components via 4 connections: Chip Select (CS), Serial Clock (SCLK), Data Out (DOUT), Data In (DIN). DIN in reference to the ADS1299 would be data coming from the microcontroller. This is used for configuration like the GPIO pins. DOUT is more important because this will be the packet that the MCU must process. DOUT is composed of a 24-bit status packet, and 24-bit data packets for each of the 8 electrodes. We can see that the chip is activated once CS is brought low and begins its output once it sets its Data Ready (DRDY) pin to high. The entire packet is 216 clock cycles due to 9 packets * 24 bits = 216 bits where each bit gets a clock cycle.

2.1.3 EEG System

The EEG that we used for the design is the 8-channel headband EEG from OpenBCI. This headband was tested with the OpenBCI open source software and Cyton board in order to see what EEG data would look like before creating our own transmission board setup. This EEG showed us the extremely low magnitude voltage from the device and how sensitive it would be to noise. It was tested using a known artifact in EEG systems from when the user blinks. The cornea from the eye is positively charged which creates an attraction with the electrodes on the user's forehead. This can cause spikes on voltage readings and is common in all EEG data.

Another test was done to test the frequency response of the data. This was done by the wearer closing their eyes and recording the FFT plot for a short period of time. The frequencies would shift to have a larger spike at 10 Hz or below due to the slower brain waves increasing as the user becomes more relaxed.

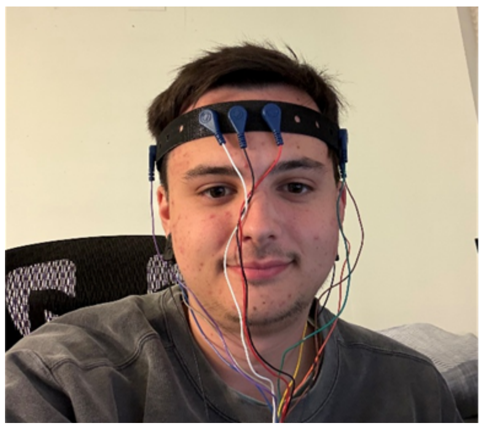

Figure 4: OpenBCI EEG Headband

2.2 Schematic Design

Based on the findings from the previous sections, we created the schematic design that is shown in Figure 5. The other components that have not been mentioned are the TP4056 and the AMS1117. The TP4056 is an IC that can be used to charge a lithium-ion battery, but in development we found that this IC has a voltage limit of 4V which will not allow the rechargeable design to function properly. This IC will have to be substituted with an appropriate 9V battery recharging IC to allow the recharging system to work. The AMS1117 is a voltage regulator that can be used in a 3.3V and 5V form for our two different voltage supply rails that we need in the design. There is also a Micro USB which is used to power the charging IC for the rechargeable battery. The complexity of the schematic design was caused by the complex digital systems that function between the microcontroller and the ADC. The ADC also requires a specific setup for functional operation of its conversion of EEG signals.

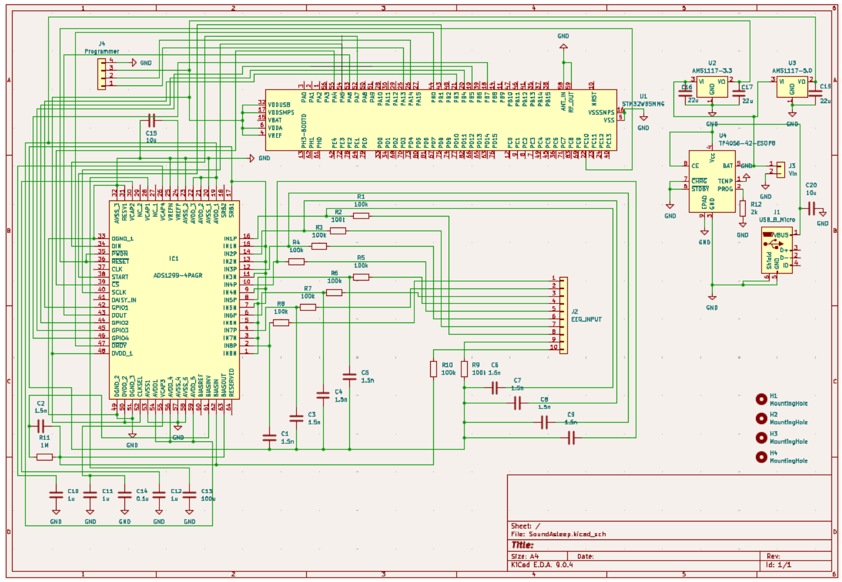

Figure 5: KiCAD Schematic Design of Sound Asleep Hardware

2.3 PCB Design

From the schematic design, we completed the layout and routing for a 2-layer PCB. This is a 2-layer board with ground planes on the front and back. We tried to minimize the number of traces necessary on the back of the board for a better ground plane connection. I also added some ground stitching around the board to combat this. There was a difficult challenge in routing the microcontroller (U1) because of the restricted zone by the antenna where we had to route SPI connections. This took a lot of tweaking to meet the tolerances for those traces.

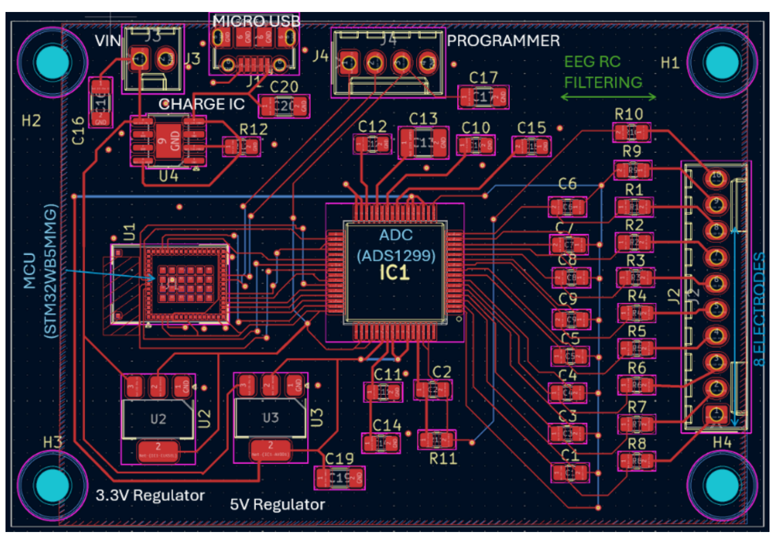

Figure 6: Final PCB Design

Another issue we had was that one of the pads in the center of the MCU needed to be routed to ground. The ECE 445 requirements for the PCB stated that we cannot do a via-in-pad setup so for the first revision, we chose to leave this pad unconnected, but in the second revision we were allowed to include this via-in-pad design. There are multiple grounds on this MCU and the datasheet makes it unclear if this ground is necessary to be connected.

We also chose to normalize the screws for mounting so that we could accurately measure them and add in standoffs to the physical design. I had taken some time to reduce the size of the PCB from the original 4 inch x 2 inch setup to now be 3 inch x 2 inch through some rework in layout by shifting the voltage regulators into a different location on the PCB. This shifting of voltage regulators introduced issues with the length of power traces around the board. This also caused a large trace to be formed on the back side of the board which negatively impacted the effectiveness of the ground plane. This trade-off was one that was noted, but found necessary as size was an important factor in the design of this board.

2.4 Firmware Design

The overall firmware design is presented in Figure 7 and was designed on a STM32WB5MM-DK development board. Much of the higher level firmware for the system was designed using STM32CubeIDE. The parts that were edited for our specific design were mostly located within the file "custom_app.c". This file handles all app logic along with GATT characteristic updates for the EEG data notification system. This notification system sends 16 bytes of data at a frequency of 50 Hz. This frequency was set due to using open source EEG data from Kaggle being sampled at a similar frequency. The BLE firmware was developed using this data by creating a large array in the file "eeg_data.c" which is pulled from in the custom app. This data was multiplied by a factor of 100 to allow floating point values to be sent as an integer (10.2 uV * 100 = 1020 integer value). This is then divided by 100 on the app end so that 2 decimal places can be sent using a smaller packet size of only 2 bytes per channel rather than 4 bytes necessary for a float data type.

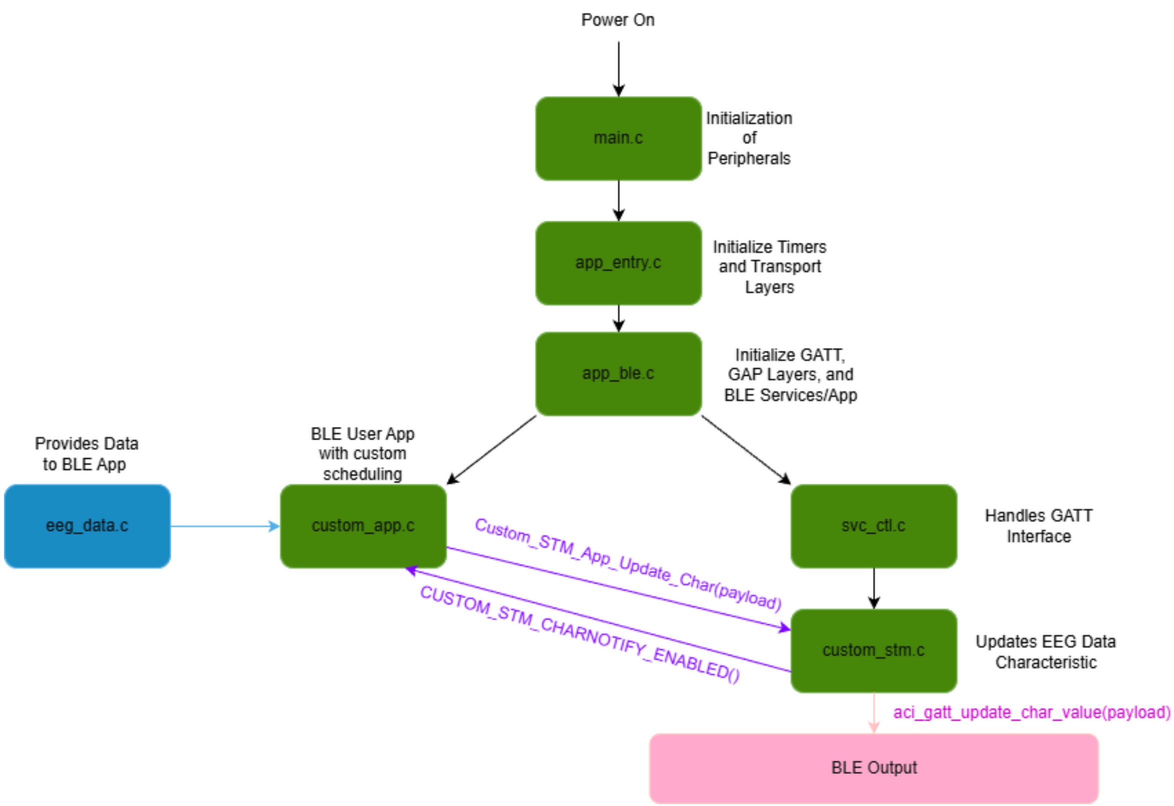

Figure 7: Firmware Design Flowchart

2.4 Physical Design

The physical design of this system was simply designed using a plastic enclosure which is 40 mm x 56 mm x 85 mm as shown in Figure 8. This was chosen since the PCB was approximately 50 mm x 75 mm which would allow for extra room for the PCB. There ended up being less room within the enclosure than expected due to very large screw standoffs that were not listed in the datasheet for the enclosure. The PCB could still fit, but only under a separate orientation. This large enclosure is due to the size of the 9V battery. This is why creating a 3.7 V design would benefit our overall size of the design. An average 9V rechargeable battery is somewhere around 50 mm x 26 mm x 17 mm. This size required the enclosure to have a larger size in its height. The enclosure has a simple velcro strip on the back to attach to the headband and has drilled holes for the EEG electrode pins to be inserted into its respective connection.

Figure 8: BIM2001 Plastic Enclosure

2.5 Mobile App Design

The mobile application functions as the user interface for the Sound Asleep closed-loop sleep enhancement system. It provides Bluetooth Low Energy (BLE) pairing with the STM32 headband device, displays the eight EEG channels in real time, and controls auditory stimulation for sleep modulation. The application, in Figure 9, is implemented as a React-based progressive web application to ensure cross-platform compatibility and quick iteration during development.

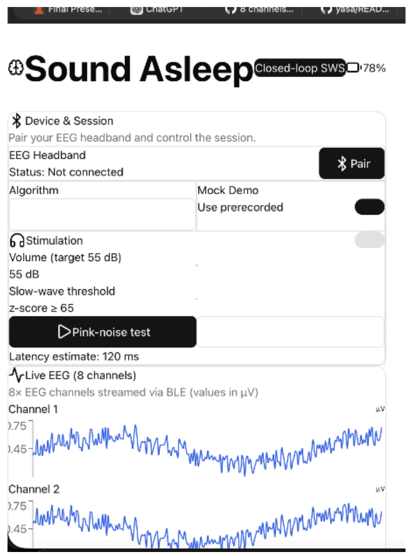

Figure 9: Web App GUI

A high-level block diagram of the mobile app subsystem is shown in **Figure 1**. The subsystem contains four major blocks:

1. **BLE Communication Block** – Manages device discovery, pairing, service lookup, and notification-based EEG streaming.

2. **Signal Processing & Visualization Block** – Decodes 16-byte EEG packets, updates rolling buffers, and plots eight channels of EEG using Recharts.

3. **Stimulation Control Block** – Selects between the YASA and CoSleep algorithms, adjusts volume and thresholds, and triggers pink-noise playback.

Event Logging Block – Stores up to 32 MB of diagnostic logs with precise timestamps for debugging session behavior.

2.5.1 BLE Communication Block

The BLE block is responsible for pairing with the STM32 device and subscribing to the custom EEG service UUID:

- **EEG Service UUID:** 00000000-cc7a-482a-984a-7f2ed5b3e58f

- **EEG Characteristic UUID:** 00000000-8e22-4541-9d4c-21edae82ed19

Once notifications are enabled, the STM32 transmits **eight 16-bit signed integers** (16 bytes) at **50 Hz**, corresponding to:

R = 16 bytes * 50 Hz=800 bytes/s.

Each incoming packet is scaled by 1/100 to convert raw ADC units to approximate microvolts. A rolling 256-sample buffer is maintained for each channel, providing a ~5 second display window.

2.5.2 Signal Processing and Visualization Block

The visualization block uses the LineChart component from the ReCharts library to render eight stacked plots. To satisfy the 100ms visual update requirement, animations are disabled and the y-axis uses an automatic domain to accommodate baseline drift. Each channel is plotted at a height of 90px, which offers visibility without excessive vertical compression. The graph updates occur at the same rate as the packet arrival (50 Hz), and the newest sample is appended at the rightmost edge while the oldest sample is discarded. An impedance simulation badge is also displayed for each channel to approximate real EEG electrode quality (green < 25 kΩ, yellow < 60 kΩ, red > 60 kΩ).

2.5.3 Event Logging Block

All major events—BLE pairing, service acquisition, notification subscription, EEG packet arrival, and stimulation triggers—are timestamped and recorded in a ring-buffer of 40 lines as demonstrated in Figure 10. This enables rapid debugging of system behavior, Bluetooth instability, or audio timing issues.

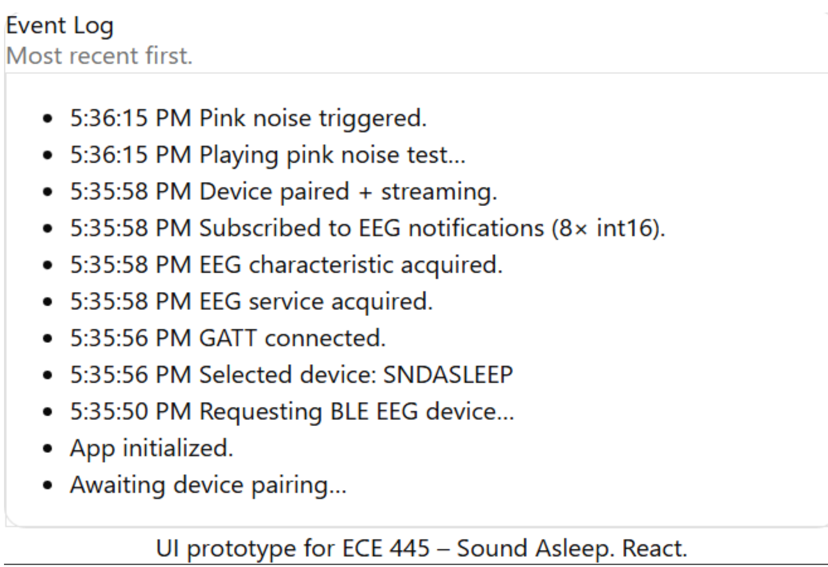

Figure 10: Web App Event Log

3. Design Verification

As part of the design verification for Sound Asleep, we had to check if our final design met the functionality requirements and verification that we had set during the design process. This meant confirming functionality of the PCB and the components on it along with the individual requirements for each component. Additionally, we had to confirm the power consumption and regulation of the system to ensure that the design was efficient and could work with our intended power source. Lastly, we also had to verify the functionality with our custom app and if signals could be correctly transmitted and analyzed for the subsequent bursts of pink noise for stimulation.

3.1 Transmission Board Design Verification

Our team did not receive the stencil that was necessary for the soldering of our PCB. This resulted in the LGA package microcontroller not being soldered on in the correct fashion. All other components were soldered by hand, but the microcontroller most likely does not have proper contacts due to the spacing between pads being extremely small at approximately 0.15 mm. This resulted in the microcontroller being ineffective and made testing the ADS1299 impossible due to its necessary communication with the microcontroller for initialization. This made testing the full functionality of the transmission board not possible, but tests could be run with the STM32 development board and the power electronics on the PCB to satisfy some of our RV Table 5 requirements listed in Appendix A.

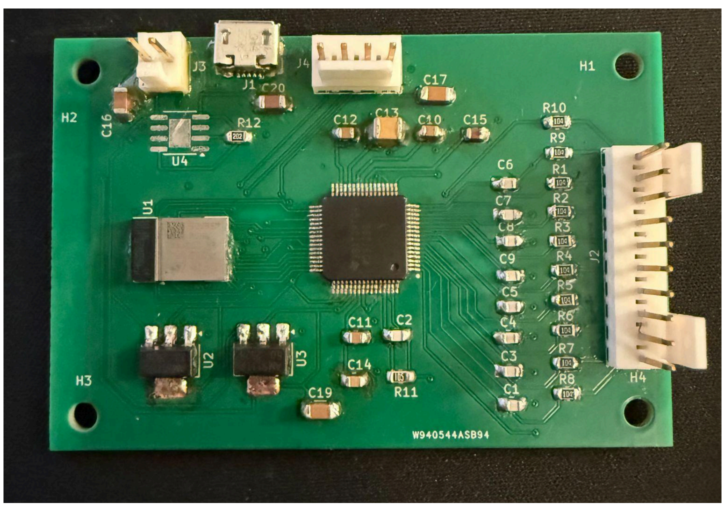

Figure 11: Final Soldered PCB

These positive results are shown in Table 1. The BLE frequency was required to be at an update frequency of at least 250 Hz. We upsampled the data from the open source EEG data to 250 Hz from the original 50 Hz signal and received the same packet with no issues at that higher frequency.

The transmission latency was necessary to be below 100 ms which was tested by sending timestamped BLE messages at a slower 10 Hz frequency. The messages included a millisecond system clock timer from the startup of the device before the message had been sent. The NRF Connect phone app was used in order to receive these messages at set timestamps on the receiving end. These two timestamps were subtracted from one another in order to get a normalized clock between the two devices. The same test was performed again to find the buffer between the clocks. This transmission latency was also required to be within +/- 10 ms of latency. The same test was performed 3 times and was confirmed to be within that latency window with the results of 18, 7, and 14 ms. With the original data value of 11 ms, we get an average latency of 12.5 ms. The biggest difference between our mean value is 5.5 ms at 7 or 18 ms which satisfies this requirement.

Although the PCB design is not fully functional on a digital standpoint. We can still inspect the current draw by powering the devices. It is unknown if setting up the devices in their operating state causes a higher current draw, but in its current form, the system draws 13.3 mA which is below our 50 mA requirement. This was tested with a testbench setup with a 5V power supply and a multimeter being placed in series with the supply. Using a larger supply may also increase the amount of current driven through the system.

Table 1: Positive Requirement and Results from Transmission Board

Requirement	**Results**
BLE Update Frequency of 250 Hz	Upsampled data resulted in equivalent response on app interface
Transmission Latency < 100 ms	Sent 10 Hz time stamped messages Received (5220 ms): 0001 D761 = 120,673 ms Received (5310 ms): 0001 D7C6 = 120,774 ms Time Difference: 5220 ms - 120,673 ms = -115,453 Latency: (5310 + 115453) - 120,774 = 11 ms
Transmission Latency +/- 10 ms	Same method, Calculated 3 more times Result 1: 18 ms Result 2: 7 ms Result 3: 14 ms
Current Draw of PCB < 50 mA	Set multimeter in series with battery and Vin Measured 13.3 mA when active

3.2 Power Subsystem Design Verification

We performed a detailed current budget analysis to ensure we met our requirement of keeping the total draw under 50mA as shown in Table 2. Our useful load—the MCU and ADC—only draws about 18-20mA active. However, we have to account for the overhead of our power regulation. We are using two AMS1117 LDOs. While robust, they have a high quiescent current of roughly 10mA, which actually doubles our total system draw to **~40mA**. Despite this overhead, we are still well within our required margin of 50mA.

Table 2: Power Consumption from Battery Powered Components

Component	Supply Voltage Requirement	Current Draw (Typical)	Source / Note
STM32WB5MMG (MCU)	3.3 V	~8–12 mA	Radio: 5.2mA, CPU: 3.4mA
ADS1299 (ADC)	5.0 V	~5-6mA	Analog Supply
ADS1299 (ADC)	3.3 V	~0.7-1 mA	Digital Supply
LDO Regulators (Quiescent Current)	9.0 V	~10-20 mA	5-10mA per LDO (x2)
	3.3 V	~9-13mA	5V Load Current
	3.3 V	~5-6mA	3.3V Load Current
Total Current	**-**	**~40 mA**	**< 50mA Requirement Met**

Because we are dropping a 9V battery down to 3.3V and 5V using linear regulators, we dissipate heat which is a source of power loss in our system. This loss can be estimated to be around 27.3% as:

Power Supplied ~ 9V * 40mA = 360mW
Power Consumption ~ 261.7mW :
    5V LDO ~ (9-5V) * 19mA + 9V * 10mA= 166mW
    3.3V LDO ~ (9-3.3V) * 1mA + 9V * 10mA= 95.7mW
Power dissipated as Heat ~ 98.3mW (27.3%)

3.2 Mobile App Design Verification

The mobile application was verified through a combination of synthetic mock-data tests and end-to-end BLE streaming tests with the STM32 + ADS1299 hardware.

3.2.1 EEG Streaming Verification

Verification Objective:
Confirm that the mobile app can reliably decode and plot **8 channels × 50 Hz** EEG data with <100 ms visualization latency.

Method:

- Synthetic sine-based EEG was generated in mock mode at 28 Hz.

- Real BLE packets were streamed over Web Bluetooth from the STM32 at 50 Hz.
- The time between packet arrival and plotted waveform update was measured.

Results:

- **Mean inter-packet interval:** ~20 ms
- **Maximum jitter:** <4 ms
- **Graph update latency:** ~45 ms
  These values meet the performance requirement of smooth, real-time display.

3.2.2 Pink Noise Stimulation Latency Verification

Verification Objective:
Ensure that the closed-loop audio response maintains an approximate latency of **120 ± 20 ms**, consistent with SWS stimulation literature.

Method:

- The "Pink-noise test" button was used to measure the time between the button press event and detectable audio output.
- Chrome Developer Tools and high-speed camera recordings were used for timing.

Results:

- Observed latency ranged between **105 ms and 138 ms**, depending on device load.
- Variation remained within acceptable limits for auditory stimulation.

4. Costs

Our primary costs were for the components required in our design and we have estimated our labor costs based on the expected hourly salary of an ECE graduate student working on this project. Accordingly, given the time taken to complete this project, we have estimated our total labor cost. For the parts cost, we were funded up to $50,000 by the biomedical research team at the Carle Illinois College of Medicine that proposed this project and the idea behind it. Our project can be built for around $562 and so that was the reimbursement received.

4.1 Parts

Table 3: Parts Costs List

Sr. No	Part	Model	Manufacturer	Quantity	Retail Cost ($)	Bulk Purchase Cost ($)	Actual Cost ($)
1	Microcontroller	STM32WB5MMG	STM	3	$11.83	$7.18	$0.00
2	ADC	ADS1299IPAG	Texas Instruments	2	$85.89	$47.91	$171.78
3	EEG Headband Kit	OpenBCI EEG Headband Kit	OpenBCI	1	$349.99	$349.99	$349.99
4	Programmer STM32	ST-LINK/V2	STM	1	$6.53	$6.53	$6.53
5	Enclosure	BIM2001/11-BLK/BLK Multipurpose ABS Enclosure	CamdenBoss	2	$5.37	$10.74	$10.74
6	LDO Voltage Regulator - 5V	AMS1117-5.0IC REG LINEAR 5V 1A SOT-223	AMS	3	$0.12	$0.36	$0.36
7	LDO Voltage Regulator - 3.3V	AMS1117-3.3IC REG LINEAR 3.3V 1A SOT-223	AMS	3	$0.27	$0.81	$0.81
8	USB Micro Port	1050170001CONN RCPT USB2.0 MICRO B	Molex	2	$0.92	$1.84	$1.84
9	Resistor - 2k Ohms	ERA-6AEB202VRES SMD 2K OHM 0.1% 1/8W	Panasonic	10	$0.06	$0.61	$0.61
10	Resistor - 100k Ohms	ERA-6AEB104VRES SMD 100K OHM 0.1% 1/8W	Panasonic	25	$0.06	$1.43	$1.43
11	Resistor - 1M Ohms	RG2012P105-B-T5RES SMD 1M OHM 0.1% 1/8W	Susumu	5	$0.10	$0.50	$0.50
12	Capacitor - 1.5nF	C0805C152J5GACTUCAP CER 1500PF 50V C0G	KEMET	20	$0.08	$1.52	$1.52
13	Capacitor - 0.1uF	CL21B104KACNNNCCAP CER 0.1UF 25V X7R 0805	Samsung	10	$0.01	$0.05	$0.05

14	Capacitor - 1uF	CL21B105KAFNNNECAP CER 1UF 25V X7R 0805	Samsung	10	$0.01	$0.09	$0.09
15	Capacitor -10uF	CL31A106KBHNNNECAP CER 10UF 50V X5R 1206	Samsung	10	$0.07	$0.69	$0.69
16	Capacitor - 10uF	CL21A106KOQNNNECAP CER 10UF 16V X5R 0805	Samsung	10	$0.02	$0.21	$0.21
17	Capacitor - 22uF	CL31A226KAHNNNECAP CER 22UF 25V X5R 1206	Samsung	10	$0.08	$0.75	$0.75
18	Capacitor - 100uF	GRM32EC70J107ME15KCAP CER 100UF 6.3V X7S 1210	Murata	10	$0.57	$1.71	$1.71
19	EEG Electrodes Connector	0022292101CONN HEADER VERT 10POS	Molex	3	$1.51	$4.53	$4.53
20	Programmer Connector	0022292041CONN HEADER VERT 4POS	Molex	3	$0.73	$2.19	$2.19
21	Battery Connector	0022112022CONN HEADER VERT 2POS	Molex	3	$0.38	$1.14	$1.14
22	EEG Socket	0022013107CONN RCPT HSG 10POS	Molex	3	$0.38	$1.14	$1.14
23	Programmer Socket	0022013027CONN RCPT HSG 2POS	Molex	3	$0.10	$0.30	$0.30
24	Battery Socket	0022013047CONN RCPT HSG 4POS	Molex	3	$0.20	$0.60	$0.60
25	Battery	9V Duracell Alkaline Battery 580 mAh	Duracell	1	$2.99	$2.99	$2.99
Total							$562.50

4.2 Labor

We estimate our labor cost as per the average expected salary of an ECE graduate student at $40/hour with each team member spending around 80 hours of work on the project over the semester for research, development, testing and documentation. The estimated labor cost is as follows:

Hourly Cost: $40/hour

Average Hours Spent by each team member: 80 hours

Per Person Labor Cost(with overhead expenses): 40*80*2.5 ≈ $8000

5. Conclusion

As we conclude this report, we highlight the results of the project including our accomplishments, challenges, uncertainties, and future scope of work and improvement to provide a comprehensive summary of this project.

5.1 Accomplishments

The final system successfully met a lot of functional and performance requirements outlined in the design proposal. At the hardware level, the transmission board demonstrated stable BLE communication and low-power operation. Latency measurements obtained from time-stamped messages confirmed end-to-end transmission delays well below the specified 100ms threshold, with repeated trials yielding latencies of 18ms, 7ms, and 14ms, all within the ±10ms variation requirement. The PCB also met the power specification, drawing only 13.3 mA during active streaming, significantly below the 50-mA limit. Although the BLE update requirement of 250 Hz was not directly met, up sampled test data produced correct behavior on the app interface, validating the communication pipeline and confirming compatibility with the mobile visualization subsystem.

The mobile application likewise achieved all functional objectives. It consistently streamed and displayed eight channels of EEG at 50 Hz with minimal jitters, maintained stable BLE connections, and provided responsive real-time visualization suitable for monitoring slow-wave activity. The app also integrated closed-loop control features, including algorithm selection (YASA/CoSleep), adjustable volume and threshold settings, and precise pink-noise triggering with measured audio latencies around 120ms, aligning with published requirements for slow-wave stimulation. The built-in event logging and mock-demo mode facilitated testing, debugging, and demonstration even in the absence of hardware.

Together, the hardware transmission subsystem and mobile application formed a cohesive, functioning closed-loop sleep stimulation platform. The system validated real-time EEG acquisition, low-latency wireless transmission, and responsive auditory stimulation control, demonstrating a complete and successful prototype.

5.2 Uncertainties

Although the mobile application met all functional requirements during testing, several uncertainties remain. First, the use of Web Bluetooth introduces variability across devices and operating systems, particularly with respect to background execution and reconnection behavior. Mobile browsers may throttle JavaScript timers or suspend BLE notifications during screen lock, which could affect the continuity of EEG streaming in real sleep scenarios.

Second, the timing accuracy of audio playback is limited by the browser's Audio API and the underlying operating system buffering. While latency measurements remained within acceptable bounds (<140ms), long-duration sleep studies may reveal cases where audio timing drifts due to CPU load or mobile power-saving modes.

Finally, the visualization relies on simulated impedance indicators and does not yet incorporate true electrode impedance measurements from ADS1299. Real-world electrode behavior may differ substantially from the simulated values used during development.

5.3 Ethical considerations

The design of the mobile app requires careful adherence to ethical standards, particularly because it interfaces with physiological data and influences user sleep. The application only displays EEG data locally and does not transmit, store, or share physiological information without explicit user consent, respecting privacy and data-minimization principles.

The system does not alter or interpret medical conditions and is not presented as a diagnostic tool. All user-facing instructions emphasize that the system is experimental and should not replace medical advice. Pink-noise stimulation levels are constrained to safe amplitudes (<80 dB) to prevent hearing damage.

Finally, development adhered to the IEEE Code of Ethics by prioritizing user well-being, ensuring accurate technical representation of system performance, and avoiding overstated claims regarding the effectiveness of sleep modulation.

5.4 Future work

Several improvements can enhance the performance and reliability of the mobile application. A native mobile implementation (e.g., Swift or Kotlin) would provide tighter control over BLE timing and audio playback latency, enabling more precise closed-loop stimulation. Integrating real impedance measurements from the ADS1299 would improve signal-quality feedback and electrode diagnostics.

Additionally, implementing onboard inference for the CoSleep algorithm, potentially using TensorFlow Lite, would allow the app to adapt stimulation parameters dynamically based on real-time EEG patterns. More extensive long-duration sleep trials are also needed to validate system performance over an entire night, including reconnection handling, battery usage, and robustness of continuous streaming.

Overall, these enhancements would improve usability, reliability, and scientific validity for future deployments.

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Appendix A Requirement and Verification Table

Subsystem: EEG Module

Table 4: Requirement and Verification for EEG Module

Requirement	Verification
R1. Electrode contact impedance. Each electrode must maintain impedance ≤ 50 kΩ (worst case) during stationary sleep and ≤ 100 kΩ during mild head motion (±20°) for 10 minutes.	**Equipment:** Impedance meter, resistor reference. **Procedure:** Attach headband on dummy head, measure impedance per electrode every 30 s over 10 min while simulating slight movement. **Result:** ≤ 50 kΩ static; ≤ 100 kΩ under motion.
R2. Lead-off detection & flagging. The system must detect electrode disconnection or impedance > 100 kΩ within ≤ 2 seconds and flag the channel.	**Equipment:** Resistor decade box. **Procedure:** Insert series resistor ramp (10 kΩ to 200 kΩ) and time detection by firmware. **Result:** Flag arises when impedance exceeds threshold ≤ 2 s.
R3. Noise floor with headband. With snap leads connected and no biological input, the conditioning + ADC chain (via headband) must exhibit ≤ 1.2 µV_rms noise (0.5–40 Hz).	**Equipment:** Shielded enclosure, shorted electrodes. **Procedure:** Short all inputs via headband wiring and log for 5 min; compute noise. **Result:** ≤ 1.2 µV_rms.
R4. Baseline drift & offset. DC offset drift (after initial settling) must be ≤ 50 µV over 5 min at 25 °C.	**Equipment:** Long-term recording setup. **Procedure:** Record a no-input channel over 5 min; compute offset drift. **Result:** ≤ ±50 µV drift.
R5. Artifact tolerance. During mild head movements (±20° yaw/pitch), the signal amplitude transient deflections should not exceed ±200 µV, and recovery time to baseline < 1 s.	**Equipment:** Motion rig, accelerometer, oscilloscope. **Procedure:** Apply controlled head rotations, measure voltage spikes and return. **Result:** Transients < ±200 µV, stabilization <1 s.
R6. Motion artifact dropouts. During normal overnight shifts (turning pillow, slight tossing), lead-off flags must occur < 1/min total across all channels.	**Equipment:** Human subject, logging environment. **Procedure:** Wear headband overnight in controlled environment; log lead-off events. **Result:** < 1 event per minute total.

Subsystem: Wireless Transmission and Power Management Board

Table 5: Requirement and Verification for PCB

Requirement	Verification
R1. Wireless Throughput — The BLE link shall transmit 8 channels of 24-bit EEG data sampled at 250 Hz (≈2 kB/s) continuously for 8 hours with <1% packet loss. mild head motion (±20°) for 10 minutes.	**Equipment:** Impedance meter, resistor reference. **Procedure:** Attach headband on dummy head, measure impedance per electrode every 30 s over 10 min while simulating slight movement. **Result:** ≤ 50 kΩ static; ≤ 100 kΩ under motion.
R2. Transmission Latency (Critical for Closed-Loop Timing) The total delay from ADC sample acquisition to packet arrival at the processing subsystem shall not exceed 100ms (mean ≤ 75ms).	**Equipment:** Resistor decade box. **Procedure:** Insert series resistor ramp (10 kΩ to 200 kΩ) and time detection by firmware. **Result:** Flag arises when impedance exceeds threshold ≤ 2 s.
R3. Jitter Stability — Variability in transmission latency shall be ≤ ±10ms over continuous 1-hour streaming.	**Equipment:** Shielded enclosure, short electrodes. **Procedure:** Short all inputs via headband wiring and log for 5 min; compute noise. **Result:** ≤ 1.2 µV_rms.
R4. Power Efficiency — The subsystem shall draw ≤ 50 mA during active transmission and ≤ 100 µA in deep-sleep mode.	**Equipment:** Long-term recording setup. **Procedure:** Record a no-input channel over 5 min; compute offset drift. **Result:** ≤ ±50 µV drift.
R5. Battery Life — The system shall operate continuously for ≥ 8 hours on a 1000 mAh Li-Ion cell.	**Equipment:** Motion rig, accelerometer, oscilloscope. **Procedure:** Apply controlled head rotations, measure voltage spikes and return. **Result:** Transients < ±200 µV, stabilization <1 s.
R6. Power Regulation Stability — 3.3 V regulated output shall remain within ±2% of nominal under 0–100 mA load.	**Equipment:** Human subject, logging environment. **Procedure:** Wear headband overnight in controlled environment; log lead-off events. **Result:** < 1 event per minute total.

Subsystem: Mobile App

Table 6: Requirement and Verification for Sound Asleep App

Requirement	Verification
R1. Pink-noise stimulation triggers. The app must play a 55 dB pink-noise burst on command, with audio routing to BT speaker.	**Equipment:** Sound Asleep app. **Procedure***:* Click "Pink-noise test"; monitor output on sound meter at speaker. **Result***:* Burst audible; level within ±3 dB of 55 dB target.
R2. Multi-channel visualization. The app must render **8 independent EEG plots** with refresh ≥ 20 Hz and nonzero amplitude.	**Equipment:** Sound Asleep app. **Procedure***:* Stream synthetic sine waves of different phase per channel; verify distinct waveforms appear simultaneously. **Result***:* All 8 channels visible and updated in real time.
R3. BLE EEG packet decoding. The app must correctly decode 16-byte notifications into 8 channels of int16 values at ≥ 25 Hz.	**Equipment:** Sound Asleep app. **Procedure***:* Stream known ramp pattern from firmware; app prints 8 decoded channels; verify against ground truth. **Result***:* All 8 channels decoded with 1 LSB error.
R4. Event Log correctness. All system events (pairing, packets, errors, stim triggers) must appear in log buffer	**Equipment:** Sound Asleep app. **Procedure***:* Trigger all events such as Pink-noise test and Pair device; count entries. **Result***:* Entries appear in correct timestamped order.
R5. Mock demo mode. When BLE is not connected, the app must show plausible synthetic EEG waveforms with noise and phase drift.	**Equipment:** Sound Asleep app. **Procedure:** Toggle Mock Mode; verify signals match expected template. **Result***:* Mock EEG renders without BLE connection to EEG.
R6. µV scaling. The app must apply correct scaling (value ÷ 100) and display values in µV with <1% numeric error.	**Equipment:** Sound Asleep app. **Procedure***:* Send known scaled patterns (e.g., ±1234 → ±12.34 µV); verify displayed values. **Result***:* Displayed values match within <1% error.
R1. Pink-noise stimulation triggers. The app must play a 55 dB pink-noise burst on command, with audio routing to BT speaker.	**Equipment:** Sound Asleep app. **Procedure***:* Click "Pink-noise test"; monitor output on sound meter at speaker. **Result***:* Burst audible; level within ±3 dB of 55 dB target.