ECE 445

SENIOR DESIGN LABORATORY

FINAL REPORT

Battery Management System for Electric Scooter

Team #35

EDWARD CHOW (ec34@illinois.edu)
JAY SUNIL GOENKA (jgoenka2@illinois.edu)
SAMAR KUMAR (sk127@illinois.edu)

TA: Xiaodong Ye

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Abstract

This paper presents the design and implementation of a Battery Management System (BMS) with integrated State of Charge (SOC) estimation and State of Health (SOH) for electric scooters. The system addresses limitations of threshold-based BMS implementations by providing real-time protection, cell balancing, and accurate capacity estimation. The BMS monitors individual cell voltages and temperatures using an LTC6811 battery monitor IC, and estimates SOC/SOH using an Open-Circuit Voltage lookup table. A 6s1p lithium-ion battery pack (22.2 V nominal, 4 Ah) serves as a scalable prototype for a full 12s design. Telemetry data is streamed via UART to an external dashboard for real-time diagnostics. Tolerance analysis indicates SOC drift from current measurement error remains below 2% under typical operating conditions. The system achieves fault response within 200 ms, SOC estimation accuracy within ±6%, and dashboard refresh rates of approximately 1 Hz, meeting all high-level requirements.

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1 Introduction

1.1 Problem

Electric scooter batteries are both safety-critical and lifecycle-critical components, as they directly affect rider safety, vehicle range, and long-term ownership costs. E-scooters are subject to frequent charge and discharge cycles, partial charging and discharging, extended storage periods, and environmental degradation. Some models also feature regenerative braking, which adds significant stress to the battery at the cost of an extended operating time. These real-world operating conditions accelerate battery degradation and increase the risk of over-discharge, over-charge, cell imbalance, or even thermal runaway if not properly managed. Given the high level of mechanical and electrical stress placed on the battery, effective management via a battery management system (BMS) is essential.

Most low-cost BMS implementations in scooters rely on fixed voltage, current, and temperature thresholds for monitoring. While these protections are necessary, threshold-based systems offer no insight into battery aging or capacity loss. As a result, battery health issues are often detected only after noticeable range decline, unexpected shutdowns while riding, or reduced charging performance-posing potential dangers to the owner.

1.2 Solution

To address the reliability and safety challenges associated with E-scooter battery systems, a Battery Management System (BMS) was developed to enable real-time monitoring, fault detection, and state estimation. The system is built around the LTC6811, which measures individual cell voltages and temperatures through direct cell taps and thermistor inputs. These measurements are communicated via isoSPI to an STM32F446, which serves as the central controller for processing and data handling.

The firmware operates on a periodic sampling framework, acquiring voltage and temperature data and evaluating it against predefined safety thresholds to detect conditions such as over-voltage, under-voltage, and thermal faults. Pack-level quantities, including total voltage and cell extrema, are computed from validated measurements to ensure robustness in the presence of erroneous readings . The processed data is then formatted and transmitted over UART to an external viewer, enabling continuous monitoring and visualization.

In addition to monitoring and protection, the system incorporates state estimation algorithms. The State of Charge (SOC) is determined using coulomb counting, with periodic correction based on an open-circuit voltage (OCV) lookup, while the State of Health (SOH) is estimated by tracking capacity degradation across discharge cycles. Together, these components provide a cohesive framework for safe and reliable battery operation, while maintaining flexibility for scaling for extended functionality.

1.3 High-Level System Functionality

- A distributed sensing architecture is employed, where a slave board measures individual cell voltages and temperatures and transmits this data to the master board for accurate, low-noise acquisition.
- The system estimates State of Charge (SOC) using coulomb counting with periodic open-circuit voltage (OCV) correction, enabling reliable tracking of remaining battery capacity over a discharge cycle.
- The master board performs centralized processing, evaluates measurements against predefined safety thresholds, and asserts fault conditions to protect the battery pack and associated electronics.
- Real-time telemetry-including cell voltages, temperatures, pack current, and system status-is streamed to an external viewer for continuous monitoring and rapid fault identification.
- The system integrates sensing, communication, estimation, and protection into a unified framework to ensure safe, reliable, and observable battery operation under varying conditions.

1.4 Block Diagram

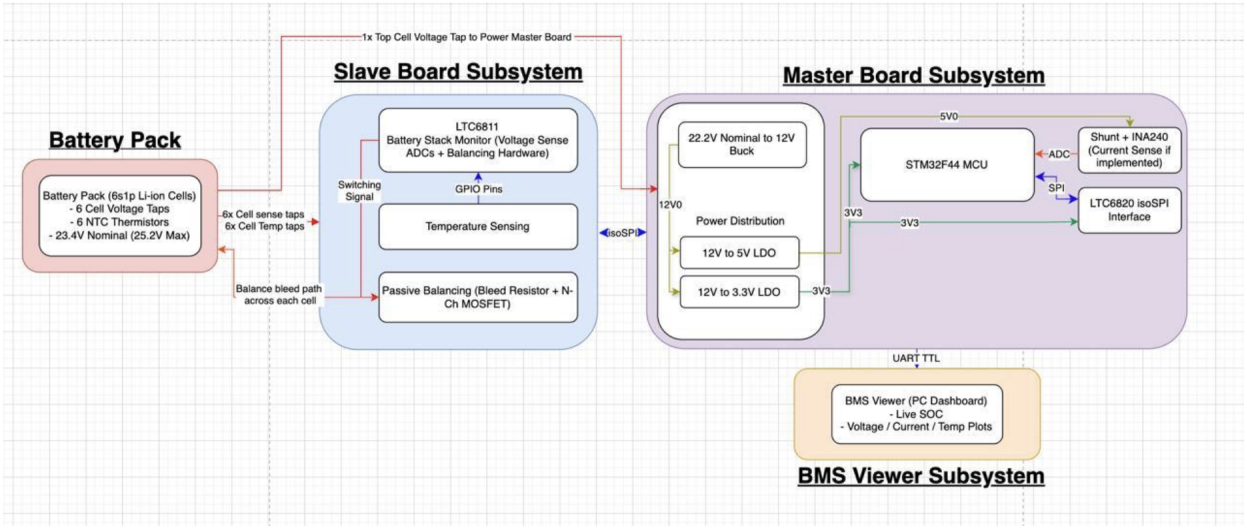

Figure 1: Block Diagram

2 Design

2.1 Subsystems Overviews and Requirements

2.1.1 Slave Board

The slave board is responsible for monitoring individual cell voltages and temperatures within the battery pack, as well as executing passive balancing. It interfaces with the master board via isoSPI communication, providing raw cell data for state-of-charge (SOC) estimation, balancing decision and fault detection to the main STM MCU.

At the heart of the slave board is the Analog Devices LTC6811 which is multi-cell battery stack monitor capable of monitoring up to 12 series connected cells with ±0.2 mV accuracy. Although the slave board is designed for a battery pack in a 6S1P configuration, the LTC6811 was chosen over the 6-channel LTC6810 to demonstrate design scalability and to gain additional auxiliary GPIO channels for temperature sensing. The LTC6811 is able to monitor cell voltages within the required voltage range of 3.0-4.2V per cell and is able to operate at a temperature range from -40°C to 125°C, making it highly suitable for e-scooter applications.

The LTC6811 can also conduct passive balancing via bleed resistors. Passive Balancing allows higher voltage cells to be discharged selectively, preventing over-voltage conditions and extending overall pack life. For temperature monitoring, six NTC thermistors (NTCALUG91A103GLA, 10 kΩ at 25°C, ±2% tolerance) are used, one per cell. To accommodate the limited number of auxiliary ADC inputs on the LTC6811 (five channels), thermistors are grouped into pairs of three. Each group feeds into an analog maximum selection circuit that outputs the highest voltage (i.e., highest temperature) from that group. This signal is then filtered and conditioned before being read by the LTC6811. As a result, all six cells are monitored for over-temperature conditions using only two auxiliary channels, with a conservative safety priority on reporting the hottest cell.

The slave board is powered directly from the lowest cell in the battery stack, allowing the LTC6811 to share the same floating reference as the cells it measures. This eliminates the need for additional isolation circuitry while maintaining accurate differential voltage measurements. The design is inherently scalable: for larger packs (e.g., 12S or multiple stacks), multiple LTC6811 devices can be daisy chained via the isoSPI interface without major architectural changes.

2.1.2 Master Board

The master board serves as the central controller of the BMS, responsible for pack level decision making, fault detection, battery isolation, SOC estimation, and external communication. It is designed around a STM32F44 microcontroller, chosen for its processing power (up to 216 MHz with FPU and DSP instructions), ample I/O for CAN/UART interfaces, and cost effectiveness.

Power for the master board is derived from the battery pack. TI's TPS54380 buck con-

verter steps down the pack voltage to a stable 12 V, accommodating the full input range from discharged to fully charged pack conditions. From this 12 V rail, two SPX1117 low dropout regulators (LDOs) generate 5 V and 3.3 V for the remaining electronics. This cascaded architecture combines the efficiency of a buck converter with the low noise output of LDOs, which is critical for sensitive analog measurements such as current sensing and ADC readings. Switching ripple from the buck converter is effectively attenuated, preserving the accuracy of SOC estimation.

The master board communicates with the slave board via isoSPI using an LTC6820 interface IC, aggregating cell voltage and temperature data from the LTC6811. SOC is estimated using a method called Coulomb counting, wherein the current flowing into and out of the battery is measured using a shunt resistor and integrated over time. The state of charge is updated based on the net charge that is transferred from/into the battery, given by:

$$SOC(t) = SOC(t_0) - \frac{1}{Q_{nom}} \int_{t_0}^{t} I(\tau)\, d\tau \tag{1}$$

where Q_{nom} is the nominal capacity of the battery and $I(t)$ is the measured current (positive for discharge and negative for charge). This method enables continuous estimation of the remaining capacity of the battery pack.

Furthermore, apart from SOC estimation, for live monitoring during maintenance or testing, the master board also streams telemetry to the BMS Viewer over a 3.3 V UART interface at 5Hz. Telemetry frames include start-of-frame bytes (0xAA, 0x55), payload length, CRC error checking, and encoded fault status flags.

Fault detection logic continuously compares measured parameters against configurable thresholds (over-voltage, under-voltage, over-temperature, over-current). Upon detecting a fault, the master board raises a BMS fault.

2.1.3 BMS Viewer

The BMS Viewer subsystem serves as the primary user interface for monitoring and diagnosing the battery management system during maintenance and testing. It acts as the final stage of the data pipeline, receiving processed telemetry from the master controller and presenting it in a structured and interpretable format. The Viewer displays all safety critical and performance relevant parameters, including individual cell voltages, total pack voltage, pack current, calculated pack power, temperature measurements, and state-of-charge (SOC).

Telemetry is transmitted from the STM32-based master board over a 3.3 V UART interface at a fixed interval of approximately 200 ms, enabling near real time updates. The firmware packages this data into structured frames with defined start-of-frame bytes (0xAA, 0x55), payload length, and CRC based error checking to ensure reliable communication . The transmitted data is derived from LTC6811 measurements and processed onboard to compute pack level quantities and extract critical information such as maximum and mini-

mum cell voltages and temperatures. These values are continuously compared against configurable thresholds (e.g., overvoltage, undervoltage, overtemperature), and the resulting fault conditions are encoded as status flags . The fault detection logic ensures that any violation of safe operating limits is captured and propagated to the Viewer for immediate visualization .

Within the Viewer, cell voltages and temperatures are displayed using bar graphs with discrete color states corresponding to normal, near threshold, and fault conditions. This visualization approach allows users to quickly identify imbalances, abnormal temperature rise, or unsafe operating conditions without interpreting raw numerical data. Pack level parameters are displayed alongside these graphs to provide a comprehensive overview of system behavior.

To maintain robustness, the Viewer performs validation on incoming telemetry frames and rejects any data that fails structural or CRC checks. Additionally, a communication timeout mechanism is implemented such that if valid data is not received within a specified interval, the Viewer flags a loss of communication condition and prevents stale data from being displayed. This ensures that all presented information reflects the current state of the system and avoids misleading diagnostics.

2.1.4 Battery Pack

The battery pack subsystem consists of a 6-series, 1-parallel (6S1P) lithium-ion configuration designed to provide the primary energy source for the system while enabling accurate monitoring and safe operation. Each cell is based on a standard 18650 lithium-ion chemistry with a nominal voltage of approximately 3.7 V and a capacity of 2200 mAh, resulting in a pack-level nominal voltage of approximately 22–23 V and a maximum voltage of 25.2 V under full charge conditions .

To support high resolution monitoring, the pack is instrumented with six direct cell voltage taps and six NTC thermistors, enabling per-cell electrical and thermal observability. This sensing architecture allows the BMS to capture critical parameters such as individual cell voltages, temperature distribution, and pack level behavior, which are essential for detecting imbalance, thermal stress, and unsafe operating conditions. The battery enclosure is electrically isolated from the pack terminals to ensure user safety and minimize the risk of unintended conduction paths .

2.2 Design Details

2.2.1 Slave Board: Passive Cell Balancing Design

The LTC6811 supports passive cell balancing per cell using a PWM duty cycle control. In the slave board, passive balancing is not only a functional requirement but also a thermal design consideration. Care was taken in component placement to ensure that a sufficient copper plane was present for heat dissipation, and the routing was designed to ensure that the discharge paths did not interfere with the integrity of the sense node. This is critical because the balancing action perturbs cell voltage, and stable, interpretable measure-

ments are required during and after balancing. The circuit for the passive cell balancing and measuring cell voltages circuit is shown below.

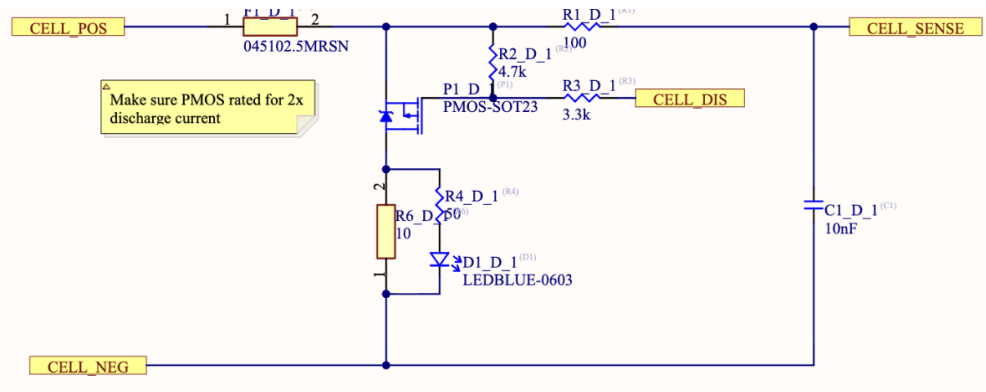

Figure 2: Passive Cell Balancing and Voltage Measurement Circuit

The design analysis is as follows:

Design Requirement: Correct an 8%–10% SOC imbalance within 1 hour for a $5\,\mathrm{Ah}$ pack.

Balancing Current Calculation:

$$I_{bal} = \frac{\%SOC_{imbalance} \cdot Q_{nom}}{t_{balance}} \tag{2}$$

$$I_{bal} = \frac{0.10 \cdot 5}{1} = 0.5\,\mathrm{A} \tag{3}$$

Discharge Resistance:

$$R_{bal} = \frac{V_{cell}}{I_{bal}} \tag{4}$$

$$R_{bal} = \frac{4.2}{0.5} = 8.4\,\Omega \tag{5}$$

The closest available resistor value was $10\,\Omega$, resulting in slightly slower balancing but still sufficient to correct approximately 8% imbalance within the required time.

Power Dissipation:

$$P = \frac{V_{cell}^2}{R} \tag{6}$$

$$P = \frac{4.2^2}{10} = 1.76\,\mathrm{W} \tag{7}$$

2.2.2 Slave Board: Initial Thermal Analysis Design Failure

Due to this relatively high power dissipation, a $3\,\mathrm{W}$ rated resistor was selected. In the first iteration of the design, even though the bleed resistor was rated for $3\,\mathrm{W}$, the high heat dissipation led to the board and nearby components heating up. This caused nearby

MOSFETs responsible for switching enabling balancing to fail. To mitigate this issue, in the second iteration of the design, multiple thermal vias were placed beneath the discharge resistor to improve heat dissipation by increasing the effective copper area. This design minimizes thermal stress on surrounding components and ensures safe operation during prolonged balancing cycles.

2.2.3 Slave Board: Temperature Sensing Design

In the battery pack, an NTC thermistor is placed on every cell and the voltage across each thermistor is monitored. Since the LTC6811 has only five auxiliary ADC inputs, directly measuring all six thermistors is not feasible. To address this, thermistors are grouped in sets of three, and each group feeds into an analog three input minimum- selection (OR-style) circuit. Each circuit outputs the lowest voltage among the three thermistors, which corresponds to the highest temperature in that group for an NTC based resistor divider. The output is filtered and conditioned before being connected to an auxiliary ADC input of the LTC6811. This approach allows all six cell temperatures to be monitored using four GPIO channels while maintaining a conservative safety strategy, as the hottest cell in each group is always reported. The circuit is shown below.

The circuit outputs the minimum voltage among inputs A, B, and C. Each input is the node voltage of a thermistor connected in a resistor divider to $5\,\mathrm{V}$, with the thermistor referenced to ground. The implementation uses an op-amp "super-diode" configuration to compensate for the forward voltage drop of the diodes, ensuring the output accurately tracks the minimum input voltage.

The design analysis is as follows:

The thermistor forms a voltage divider with a fixed resistor, and the node voltage is given by:

$$V_{out} = V_{ref} \cdot \frac{R_{NTC}}{R_{fixed} + R_{NTC}} \tag{8}$$

For an NTC thermistor, the resistance varies with temperature as:

$$R_{NTC}(T) = R_0 \cdot e^{\beta\left(\frac{1}{T} - \frac{1}{T_0}\right)} \tag{9}$$

Thus:

$$T \uparrow \Rightarrow R_{NTC} \downarrow \Rightarrow V_{out} \downarrow \tag{10}$$

This establishes that the lowest voltage corresponds to the highest temperature.

The output of the circuit is therefore:

$$V_{out} = \min(V_A, V_B, V_C) \tag{11}$$

which corresponds to:

$$T_{out} = \max(T_1, T_2, T_3) \tag{12}$$

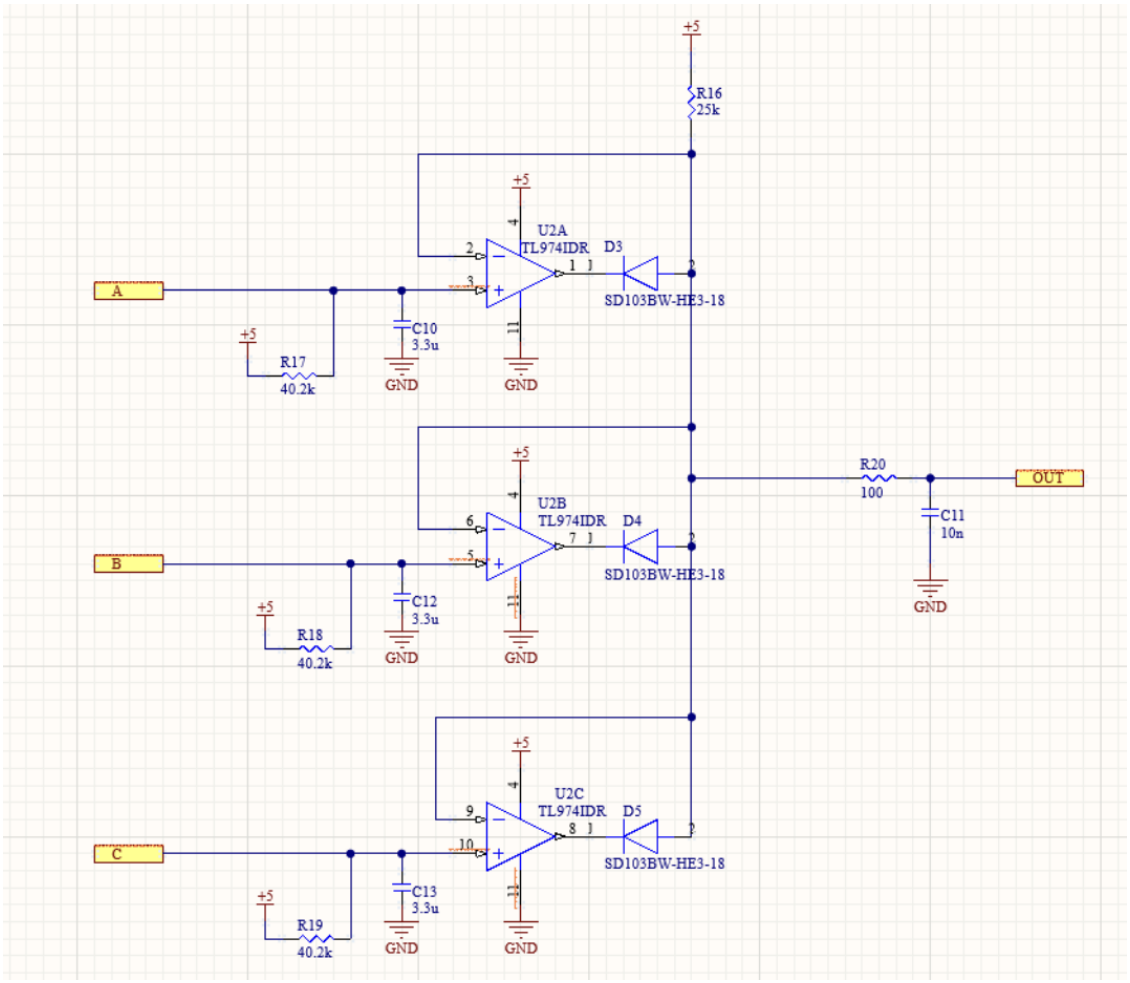

Figure 3: Slave Board: Temperature Sensing Circuit

Stage 1 – Precision Active Rectification: The input stage uses the TL974 op-amp with a Schottky diode placed inside the feedback loop. This allows the op-amp to compensate for the diode forward voltage drop and enables precise voltage tracking.

Stage 2 – Minimum Selection ("Lowest Wins"): The common bus is pulled up to $5\,\mathrm{V}$ via a $25\,\mathrm{k}\Omega$ resistor. The op-amp whose non-inverting input has the lowest voltage drives the bus low by sinking current. The bus voltage therefore equals the lowest input voltage.

Stage 3 – Diode Blocking: When one op-amp clamps the bus to the lowest input voltage, the remaining op-amps see a lower voltage at their inverting inputs than at their non inverting inputs. This forces their outputs high, effectively isolating them and preventing interference with the selected minimum signal.

2.2.4 Master Board: Current Sensing Design

To monitor current and calculate SOC of the pack, initially the OCV lookup method was chosen. However, after the feedback from the design review, it was realized that it would

be more accurate and better for the purpose of real life relevance of the project if SOC was estimated using a shunt resistor instead of OCV lookup method. This required a significant redesign of the master board because the OCV lookup method did not require any additional hardware but the shunt resistor method for current sensing required a low drift voltage amplifier.

Initially, the AMC1301 was chosen as the low drift voltage amplifier, as that would also provide galvanic isolation along voltage amplification. This was based on the assumption that for a 12S1P 60V pack wherein the design would require galvanic isolation and separation of measurement domain from the control domain.

However, once the scope of the project was reduced from 6S to 12S, the AMC1301 was replaced it with a direct high side current sense amplifier as galvanic isolation was no longer needed for voltages below 50V. The high side current sense amplifier used in the design is the TI's INA240 with a 100V/V gain.

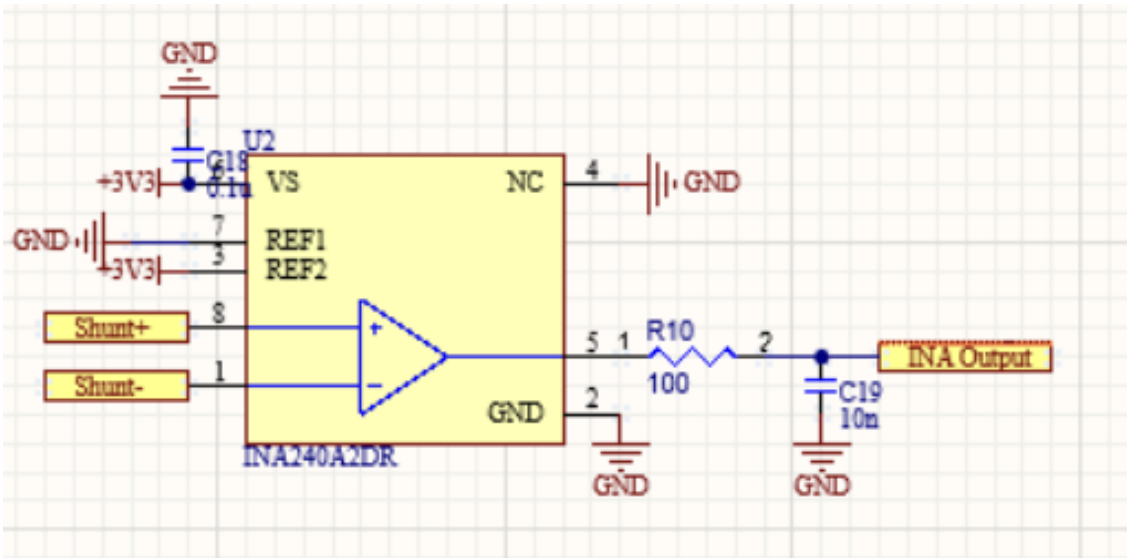

Figure 4: Master Board: Current Sensing Circuit

The design is low-side current sensing configuration in which the shunt resistor is placed between the battery pack ground and system ground. This allows for a simple measurement circuitry where the design does not need a high common-mode voltage handling in the amplifier with a charge boost.

More specifically, TI's INA240 was used in the design as it features a low gain error and offset drift, which are critical for accurate current measurement. Since SOC estimation via coulomb counting integrates current over time, even small offset errors can accumulate and result in significant SOC estimation inaccuracies in the long run.

Additionally, the INA240 is able to provide enhanced PWM rejection and is specifically designed for high common-mode transient environments.. This was a core requirement for our design as the master board has a switching regulator, which can introduce noise and transients into the system.

In all, this combination of low offset, low gain drift, and high noise rejection made the INA240 very suitable for accurate and reliable current sensing.

For the current sensing design, a $1\,\mathrm{m}\Omega$ shunt resistor with a $100\,\mathrm{V/V}$ gain on the amplifier was chosen. Our design is specified for a $5\,\mathrm{A}$ minimum current and $30\,\mathrm{A}$ maximum current. This means that using Ohm's law:

$$\text{Max Shunt Voltage} = I \cdot R = 0.001\,\Omega \cdot 30\,\mathrm{A} = 30\,\mathrm{mV} \tag{13}$$

$$\text{Min Shunt Voltage} = 0.001\,\Omega \cdot 5\,\mathrm{A} = 5\,\mathrm{mV} \tag{14}$$

After the amplification, the ADC configured pin on the STM MCU would read:

$$\text{Max ADC Input Voltage} = G \cdot \text{Shunt Voltage} = 30\,\mathrm{mV} \cdot 100 = 3\,\mathrm{V} \tag{15}$$

$$\text{Min ADC Input Voltage} = 5\,\mathrm{mV} \cdot 100 = 0.5\,\mathrm{V} \tag{16}$$

As the STM32 ADC range is $0\,\mathrm{V}$ to $3.3\,\mathrm{V}$, the design is able to utilize most of the range without any saturation leading to higher resolution.

Furthermore this design is able to resolve approximately $8\,\mathrm{mA}$ as derived from the following equations:

$$\text{ADC LSB} = \frac{3.3}{4096} = 0.8\,\mathrm{mV} \tag{17}$$

$$\text{ADC LSB in reference to } V_{\text{shunt}} = \frac{0.8\,\mathrm{mV}}{100} = 8\,\mu\mathrm{V} \tag{18}$$

Therefore,

$$\text{Equivalent Current Resolution} = \frac{8\,\mu\mathrm{V}}{1\,\mathrm{m}\Omega} = 8\,\mathrm{mA} \tag{19}$$

A resolution of $8\,\mathrm{mA}$ is a high-resolution current measurement and suitable for accurate SOC estimation using coulomb counting for the design specification.

2.2.5 Master Board: Power Tree Design

The master board takes in pack voltage ($18\,\mathrm{V}$ to $25.2\,\mathrm{V}$) as input and using a buck converter, first steps it down to $12\,\mathrm{V}$. The $12\,\mathrm{V}$ is then further regulated to $5\,\mathrm{V}$ and $3.3\,\mathrm{V}$ via linear regulators. The $5\,\mathrm{V}$ and $3.3\,\mathrm{V}$ rails are used to power all components on the master board including the MCU.

The TPS54308 buck converter was selected as it is a buck converter with synchronous rectification and is able to accept a variable input voltage from $4\,\mathrm{V}$ to $36\,\mathrm{V}$ and convert it to $12\,\mathrm{V}$. It also required a relatively low-valued and small sized inductor which helped reduce the size of the board and BOM cost. Furthermore, linear regulators were not used to step down pack voltage to $3.3\,\mathrm{V}$ and $5\,\mathrm{V}$ as linear regulators dissipate the difference in voltage as heat. This would lead to huge inefficiencies and significant heat generation.

Linear regulators, instead, were used to step down the voltage from $12\,\mathrm{V}$ to $3.3\,\mathrm{V}$ and $5\,\mathrm{V}$. The SPX1117 LDO regulator in this design is an $800\,\mathrm{mA}$ class low dropout voltage regulator. It is employed in applications where low-noise voltage rails are required after the buck pre-regulator and when there is a need for compactness, cost effectiveness, and moderate current drive capacity. It provides low-noise voltage rails and high ripple rejection, which is required in analogue and digital measurement applications, as in this case on the master board. For both $5\,\mathrm{V}$ and $3.3\,\mathrm{V}$ voltage rails, several $1\,\mu\mathrm{F}$ capacitors along with TVS diodes were also used as bypass and decoupling capacitors.

Justification for Using Buck Converter over LDO:

For a linear regulator, the power dissipated as heat is given by:

$$P_{loss} = (V_{in} - V_{out}) \cdot I_{load} \tag{20}$$

Assuming worst-case input voltage:

$$V_{in} = 25.2\,\mathrm{V}, \quad V_{out} = 12\,\mathrm{V} \tag{21}$$

$$P_{loss} = (25.2 - 12) \cdot I_{load} = 13.2 \cdot I_{load} \tag{22}$$

For a modest load current of $1\,\mathrm{A}$:

$$P_{loss} = 13.2\,\mathrm{W} \tag{23}$$

This is a lot high thermal dissipation which makes an LDO impractical due to excessive heat generation and poor efficiency.

Efficiency of an LDO is given by:

$$\eta_{LDO} = \frac{V_{out}}{V_{in}} \tag{24}$$

$$\eta_{LDO} = \frac{12}{25.2} \approx 47.6\% \tag{25}$$

In contrast, however, the buck converter, TPS54308, in our design typically operates at efficiency of 85%–95%, significantly reducing power loss and thermal stress.

Therefore, a buck converter is used for the initial step-down from pack voltage to $12\,\mathrm{V}$, followed by LDOs for final regulation where low noise is required.

2.2.6 Master Board: Initial Buck Failure Design Analysis

In the first round design, the buck converter did not perform as expected as an incorrect inductor value was chosen. As explained before, the buck converter was designed to step down from a worst case input of $25.2\,\mathrm{V}$ to $12\,\mathrm{V}$ at a switching frequency of $500\,\mathrm{kHz}$. An inductor value of $4.7\,\mu\mathrm{H}$ as initially selected led to an excessive inductor current ripple on the 12V rail.

The inductor current ripple is given by:

$$\Delta I_L = \frac{V_{out}(1-D)}{L \cdot f_s} \tag{26}$$

where $D = \frac{V_{out}}{V_{in}} = \frac{12}{25.2} \approx 0.476$.

Substituting values:

$$\Delta I_L = \frac{12 \cdot (1-0.476)}{4.7 \times 10^{-6} \cdot 500 \times 10^3} \approx 2.67\,\mathrm{A} \tag{27}$$

For a nominal load current of $2\,\mathrm{A}$, this ripple is larger than the average current, meaning:

$$I_{L,avg} < \frac{\Delta I_L}{2} \tag{28}$$

which forces the converter into discontinuous conduction mode (DCM). When operating in DCM, the current of the inductor falls to 0 during a part of the switching cycle. This results in an increased output voltage ripple, reduced efficiency, and poor load regulation.

The output voltage ripple can be approximated as:

$$\Delta V_{out} \approx \frac{\Delta I_L}{8 \cdot f_s \cdot C_{out}} \tag{29}$$

which increases significantly with higher ΔI_L, leading to instability in downstream voltage rails.

To resolve this, the inductor value was increased to $10\,\mu\mathrm{H}$, reducing the ripple current to:

$$\Delta I_L \approx 1.25\,\mathrm{A} \tag{30}$$

This ensured operation in continuous conduction mode (CCM), improving output stability, reducing ripple, and enhancing overall converter efficiency.

2.2.7 Communication Protocol Selection (isoSPI and SPI)

Communications between the master and slave boards are carried out using isoSPI technology, while SPI is used locally between the MCU and the interface. The reason for choosing these protocols is their reliability, resistance to noise, and scalability.

The LTC6811 has built-in support for isoSPI communication and is a differential communication method designed specifically for high voltage battery packs. Through the use of differential signaling and transformer isolation, signals can travel long distances while remaining resistant to noise in high voltage environments.

There is significant electromagnetic interference (EMI) in a battery pack environment due to switching regulators, balancing circuits, and load transients. isoSPI addresses these challenges through:

- Differential signaling, which improves common mode noise rejection
- Transformer based isolation, enhancing electrical safety and breaking ground loops

Thus, isoSPI ensures isolated and robust communication between the master and slave boards, while SPI enables fast and reliable local communication.

3 Design Verification

3.1 Slave Board Verification

Requirement and Acceptance Criteria	**Verification Procedure**	**Result**
The slave board shall conduct passive balancing with discharge current ≥ 20 mA per cell at 4.2 V.	Apply 4.2 V to the cell input using a bench supply, enable balancing, and measure discharge current with a DMM.	22.4 mA measured (≥ 20 mA requirement satisfied).
The slave board shall measure cell temperatures within ± 4°C of thermocouple reference readings.	Record LTC6811 temperature readings and compare them to thermocouple measurements.	Maximum error = 1.8°C (within ± 4°C requirement).
The slave board shall measure cell voltages from 3.0 V to 4.2 V within ± 10 mV of reference readings.	Apply 3.0 V, 3.7 V, and 4.2 V using a precision supply, record LTC6811 readings, and compare to a 6.5-digit DMM.	Maximum error = 6.2 mV (within ± 10 mV requirement).
The max-selection circuit shall output the highest of three thermistor input voltages.	Apply three distinct voltages using programmable voltage sources, measure the output, and repeat for input permutations.	Output matched highest input for all permutations (100% correctness).

Table 1: Slave Board Verification Results

3.2 Main Board Verification

The main board was validated to ensure proper power regulation, reliable communication, accurate sensing, and correct fault handling.

Requirement	Verification	Result
The main board shall generate 12 V, 5 V, and 3.3 V rails within $\pm$5% of nominal values from a $\sim$23 V input.	Power the board using a battery pack or bench supply and measure each rail using a calibrated digital multimeter.	Pass: 12.08 V, 5.02 V, 3.31 V (all within tolerance).
The STM32 shall successfully flash and execute firmware, confirmed via LED heartbeat and UART output at 115200 baud.	Flash firmware using ST-LINK and STM32CubeIDE. Verify LED heartbeat and UART startup message.	Pass: Firmware executed correctly with stable UART at 115200 baud.
UART telemetry shall transmit at $\geq$10 Hz with valid CRC and no observed packet corruption.	Connect UART to a PC terminal or BMS Viewer and monitor telemetry frames.	Pass: Stable 10 Hz transmission with valid CRC and no corruption observed.
The INA current measurement shall report values within $\pm$5% of DMM reference measurements.	Apply known load currents and compare UART-reported current with DMM readings.	Pass: 2.01 A measured vs 1.97 A reported ($<$5% error).
The LTC6820 shall generate valid SPI/isoSPI communication with SPI operating at 1 MHz.	Send LTC6811 commands and probe SPI/isoSPI lines using an oscilloscope or logic analyzer.	Pass: 1 MHz SPI operation with valid isoSPI signaling confirmed.
isoSPI communication with the LTC6811 shall complete at least 500 read cycles with 0 PEC/CRC errors.	Trigger LTC6811 conversions and read voltage/temperature data over isoSPI.	Pass: 0 CRC errors observed over 500 cycles.
The BMS fault output shall assert low within $\leq$20 ms under OV, UV, OC, or communication fault conditions.	Inject fault conditions and monitor the fault output using a DMM or oscilloscope.	Pass: Fault asserted low within 20 ms for all tested conditions.

Table 2: Main Board Requirements, Verification, and Results

3.3 BMS Viewer

The BMS Viewer subsystem was validated to ensure reliable telemetry visualization, fault indication, and simulation capability.

Requirement	Verification	Result
The BMS Viewer shall parse STM32 UART packets with $\geq$99% accuracy and reject invalid packets using SOF, length, and CRC.	Connect the viewer to the STM32 UART stream. Verify that packets with correct SOF, payload length, and CRC are accepted. Ensure parsed fields populate correctly in the UI.	Packet parsing accuracy observed at $>$99%; all invalid packets correctly rejected.
The BMS Viewer shall update telemetry at $\geq$1 Hz with no noticeable lag or dropouts.	Run the system and observe live telemetry updates. Record timestamps from the viewer or logs. Confirm updates occur at $\geq$1 Hz.	Telemetry update rate measured at $\sim$1.1 Hz with continuous updates and no visible dropouts.
The BMS Viewer shall visually indicate OV, UV, OT, and OC faults within $\leq$500 ms using distinct indicators.	Run the viewer with live or simulated telemetry. Introduce fault conditions through firmware flags or simulation mode. Verify that each fault maps to a distinct visual indicator.	All fault conditions were correctly indicated within $\sim$300–500 ms.
The BMS Viewer shall return to normal state within $\leq$1 s after fault clearance.	Clear the fault condition and confirm that the UI returns to the normal state.	UI returned to normal within $\sim$1 s with no residual fault indicators.
The BMS Viewer shall support simulated BMS telemetry packets for demo/debug mode with stable operation and realistic ranges.	Enable simulation mode without hardware. Generate synthetic packets. Verify that the UI updates like live hardware mode and switching modes does not crash the viewer.	Simulation mode operated reliably; switching between modes showed no crashes or data corruption.

Table 3: BMS Viewer Requirements, Verification, and Results

3.4 Battery Pack

The battery pack subsystem was validated to ensure correct pack voltage, continuous discharge capability, and electrical isolation from the enclosure.

Requirement	Verification	Result
The battery pack subsystem shall supply 23.4 V nominal ±5% under normal operating conditions and shall not exceed 25.2 V at full charge when no fault condition is present.	Ensure the battery pack is fully assembled and not connected to the BMS fault circuitry. Measure the output voltage across the pack terminals using a calibrated digital multimeter at full SOC and mid SOC. Confirm the measured voltage remains within the required range and does not exceed 25.2 V at full charge.	Pack voltage remained within the required range during testing; full-charge voltage did not exceed 25.2 V.
The battery pack subsystem shall deliver a continuous discharge current of at least 2 A without the pack voltage dropping more than 10% below nominal voltage during steady-state operation.	Connect the battery pack to a programmable electronic load and set the discharge current to 4 A for 60 seconds. Measure steady-state voltage and confirm that voltage remains at or above 19.78 V. Verify that no abnormal heating, instability, or connection failure occurs during the test.	Pack successfully delivered 4 A for 60 seconds; voltage remained above 19.78 V with no abnormal heating, instability, or connection failure.
The battery pack subsystem shall maintain electrical isolation between the battery terminals and the enclosure with insulation resistance of at least 1 MΩ.	Disconnect the battery pack from the BMS and all external electronics. Measure the insulation resistance between the positive terminal and enclosure, and between the negative terminal and enclosure, using a multimeter or insulation tester.	Both terminal-to-enclosure insulation resistance measurements were greater than 1 MΩ; no unintended conductive path was observed.

Table 4: Battery Pack Requirements, Verification, and Results

4 Cost & Schedule

4.1 Cost

Cost of Labor:

We assume a labor salary of $45/hour and estimate that each partner roughly puts in 7 hours/week on average. Given that there were around 15 full weeks this semester, total labor cost comes out as follows:

Person	Rate ($/hr.)	Multiplier	Weeks	Hours/Week	Total Hours	Total Cost ($)
Samar	45	2.5	15	7	105	11,812.00
Edward	45	2.5	15	7	105	11,812.00
Jay	45	2.5	15	7	105	11,812.00
Total	–	–	–	–	315	35,436.00

Cost of Components:

Description	Manufacturer	Part #	Qty.	Price
Battery Cells	Auline	VTC6 18650	1	$70
Microcontroller	STMicroelectronics	STM32F446RET6TR	1	$8.12
Battery Monitor IC	Analog Devices	LTC6811-1	1	$23.35
Operational Amplifier	Texas Instruments	TL974IDR	4	$4.18
NPN Transistor	onsemi	BCP56T3G	3	$1.95
P-Channel MOSFET	Infineon Technologies	BSS308PEH6327XTSA1	20	$5.46
N-Channel MOSFET	Diodes Incorporated	BSS123TA	5	$2.40
Schottky Diode	Vishay	SD103BWS-E3-18	20	$3.14
Ceramic Capacitor	KEMET	C0603C103K5RACTU	25	$0.23
Resistor	Yageo/Bourns	Multiple	50	$8
Header	Semtec	IPL1-109-01-L-D-K	6	$16
Transformer	Pulse Electronics	HM2113ZNL	3	$13
Iso/SPI Communication	Analog Devices	LTC6820	1	$8
Thermistor	Vishay	NTCALUG91A103GL	6	$12
Current Amplifier	Texas Instruments	INA240	1	$4
Shunt Resistor	Vishay Dale	RCWE1206R226FKEA	1	$2
Power MOSFET	Infineon Technologies	IPP030N10N5XKSA1	2	$10
Gate Driver	Microchip Technology	MCP1416T-E/OT	1	$1

Total Cost:

The total cost of the parts and labor is:

$$\$175.83 + \$35{,}436 = \$35{,}611.83$$

4.2 Schedule

Week	Task	Person
2/23 – 3/1	Master PCB routing and design review preparation	Samar
	Initial STM32 firmware framework (SPI, UART, GPIO)	Edward
	Initial BMS Viewer structure (data parsing mock inputs)	Jay
	Finalize Design Document submission	Everyone
3/2 – 3/8	Incorporate Design Review feedback into PCB + Breadboard Demo Preparation	Samar
	Complete Master PCB layout and DRC checks	Samar
	Implement isoSPI firmware base driver	Edward
	Implement live plotting framework in Viewer	Jay
3/9 – 3/15	Breadboard Demo milestone	Everyone
	Finalize Slave PCB layout and order PCBs	Samar
	Implement current sensing driver (INA240 + ADC)	Edward
	Implement serial communication parser (UART)	Jay
3/16 – 3/22	**Spring Break**	-
3/23 – 3/29	Assemble Master and Slave PCBs	Samar
	Bring up power rails (buck + LDO validation)	Samar
	Validate SPI + isoSPI communication stack	Edward
	Display live voltage data in Viewer	Jay
3/30 – 4/5	Debug PCB issues and order revision if needed	Samar
	Implement Coulomb Counting SOC algorithm	Edward
	Implement temperature visualization and alert display	Jay
4/6 – 4/12	Progress Demo milestone	Everyone
	Validate passive balancing hardware (≥20 mA)	Samar
	Implement MOSFET fault disconnect control (<200 ms)	Edward
	Integrate real-time data refresh (~1 Hz)	Jay
4/13 – 4/19	Final PCB debugging and stability testing	Samar
	Validate SOC accuracy within ±6%	Edward
	Implement fault indication (OV, UV, OC, OT) in Viewer	Jay
4/20 – 4/26	Mock Demo milestone	Everyone
	Full system integration testing	Everyone
4/27 – 5/3	Final Demo and Presentation	Everyone
5/4 – 5/10	Final Paper and Lab Checkout	Everyone

Figure 5: Schedule

5 Conclusion

5.1 Accomplishments and Uncertainities

This project successfully demonstrated a functional battery management system for a 6S1P lithium-ion electric scooter battery pack. The final system integrated cell voltage sensing, temperature monitoring, passive balancing, current measurement, fault detection, SOC/SOH estimation, isoSPI communication, and UART telemetry. The master board generated 12 V, 5 V, and 3.3 V rails within $\pm 5\%$, transmitted valid telemetry at 10 Hz, and completed 500 isoSPI read cycles with 0 CRC errors. The slave board measured cell voltages with a maximum error of 6.2 mV, measured temperature with a maximum error of 1.8°C, and achieved 22.4 mA passive balancing current at 4.2 V. The BMS Viewer updated telemetry at approximately 1.1 Hz and correctly displayed system fault states.

Although the system met its primary requirements, some uncertainties remain. SOC estimation was achieved within approximately $\pm 6\%$, but it was not fully characterized across long-term aging, wide temperature variation, or repeated charge-discharge cycles. Current sensing was verified using representative loads, including a 2.01 A DMM reference and 1.97 A reported value, but additional testing across a wider scooter load profile would improve confidence. Passive balancing also creates localized heating, since the 10 Ω bleed resistor dissipates approximately 1.76 W at 4.2 V, so longer thermal testing would be needed before production use.

5.2 Future Work and Alternatives

Future work should focus on improving field readiness and scalability. The prototype was implemented for a 6S1P pack, but the LTC6811 architecture can be extended toward a 12S scooter battery system. Additional work should include higher-current pack testing, long-duration cycling, enclosure-level thermal validation, and integration with a contactor or solid-state disconnect for pack isolation. SOC/SOH estimation could also be improved using temperature compensation, measured-capacity calibration, or a more advanced battery model. A possible design alternative is active balancing, which would reduce wasted energy and heat but increase circuit complexity and cost.

5.3 Ethical Considerations

Ethical and safety considerations were central to this project because lithium-ion battery systems can create risks such as thermal runaway, high-current faults, unsafe temperature rise, and unexpected shutdowns. In accordance with the IEEE Code of Ethics, the design prioritized public safety through overvoltage, undervoltage, overcurrent, overtemperature, and communication fault detection, with the BMS fault output asserting low within 20 ms during testing. The system also improves reliability by giving users accurate information about battery condition, which can reduce unsafe operation, extend battery lifetime, lower ownership cost, and decrease electronic waste.

References

[1] Analog Devices, "LTC6811-1/LTC6811-2 Multicell Battery Stack Monitor Datasheet," Analog Devices, 2023.

[2] Analog Devices, "LTC6820 isoSPI Isolated Communications Interface Datasheet," Analog Devices, 2022.

[3] Texas Instruments, "INA240 Precision Bidirectional Current-Sense Amplifier Datasheet," Texas Instruments, 2023.

[4] STMicroelectronics, "STM32F446xx ARM Cortex-M4 Microcontroller Datasheet," STMicroelectronics, 2023.

[5] Texas Instruments, "TPS54308 4.5-V to 28-V Input, 3-A Synchronous Step-Down Converter Datasheet," Texas Instruments, 2022.

[6] MaxLinear, "SPX1117 Low Dropout Voltage Regulator Datasheet," MaxLinear, 2021.

[7] Texas Instruments, "TL974 Quad Low-Noise Operational Amplifier Datasheet," Texas Instruments, 2022.

[8] Vishay Intertechnology, "NTCALUG Series Thermistor Datasheet," Vishay, 2021.

[9] W. Waag, C. Fleischer, and D. U. Sauer, "Critical review of the methods for monitoring of lithium-ion batteries in electric and hybrid vehicles," *Journal of Power Sources*, vol. 258, pp. 321–339, 2014.

[10] G. L. Plett, "Extended Kalman filtering for battery management systems of LiPB-based HEV battery packs: Part 1. Background," *Journal of Power Sources*, vol. 134, no. 2, pp. 252–261, 2004.

[11] B. Scrosati and J. Garche, *Lithium Batteries: Advanced Technologies and Applications*. Hoboken, NJ, USA: Wiley, 2013.

[12] M. Daowd, N. Omar, P. Van Den Bossche, and J. Van Mierlo, "Passive and active battery balancing comparison based on MATLAB simulation," in *Proc. IEEE Vehicle Power and Propulsion Conf.*, 2010, pp. 1–7.

[13] International Electrotechnical Commission, "IEC 62619: Secondary cells and batteries containing alkaline or other non-acid electrolytes – Safety requirements for secondary lithium cells and batteries," IEC Standard, 2022.

[14] J. Axelson, *Serial Port Complete: COM Ports, USB Virtual COM Ports, and Ports for Embedded Systems*, 2nd ed. Madison, WI, USA: Lakeview Research, 2007.

[15] IEEE, "IEEE Code of Ethics," 2020. [Online]. Available: https://www.ieee.org/about/corporate/governance/p7-8.html

Appendix A Battery Pack Subsystem

A.1 Assembled Battery Pack

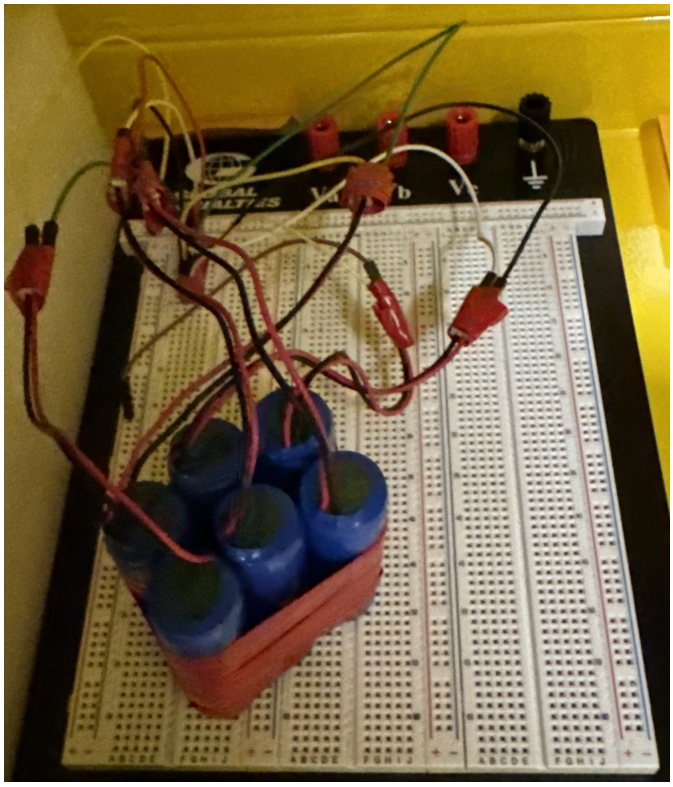

Figure 6: Battery Pack

Appendix B Slave Board Subsystem

B.1 PCB Schematic for the Slave Board

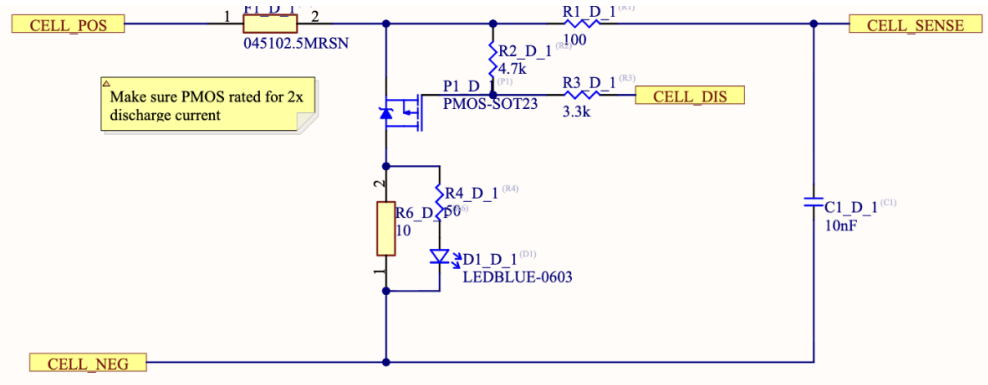

Figure 8: Passive Balancing and Voltage Measurement Circuit

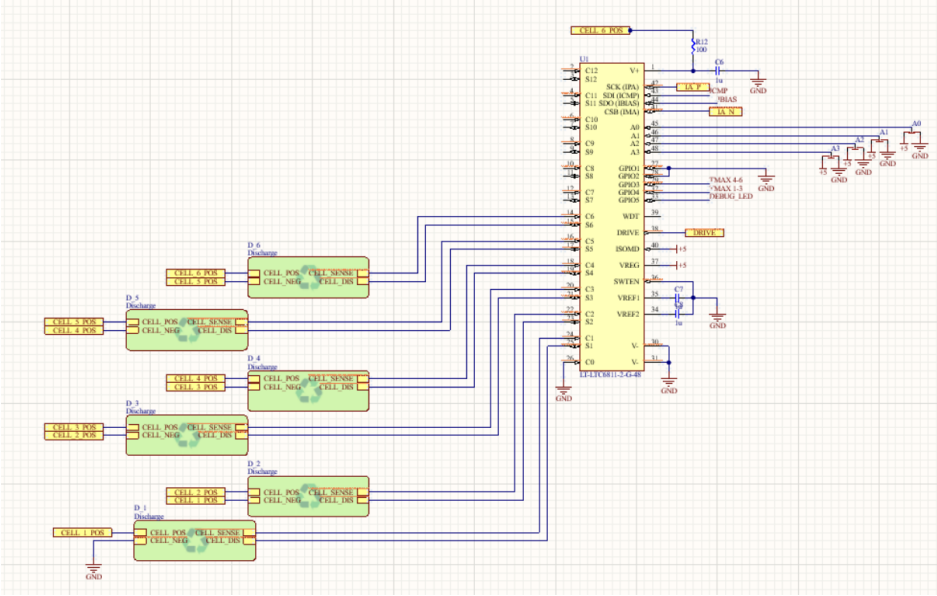

Figure 7: LTC6811 Circuit

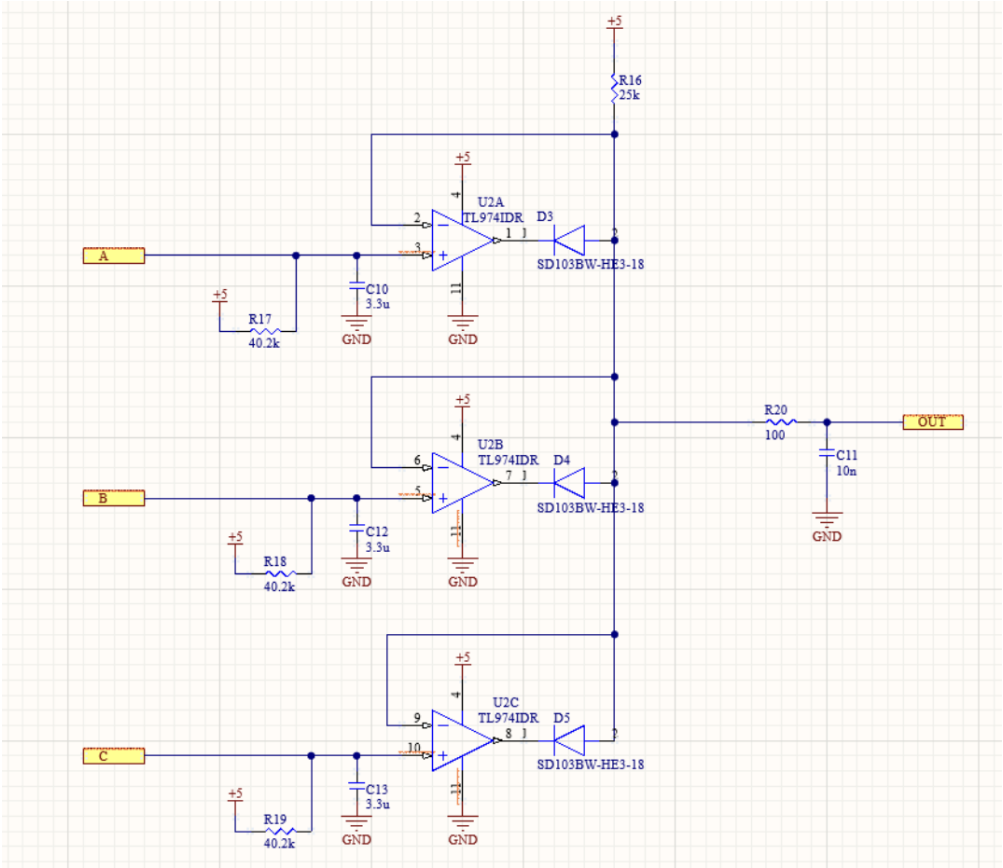

Figure 9: Temperature Sensing Circuit

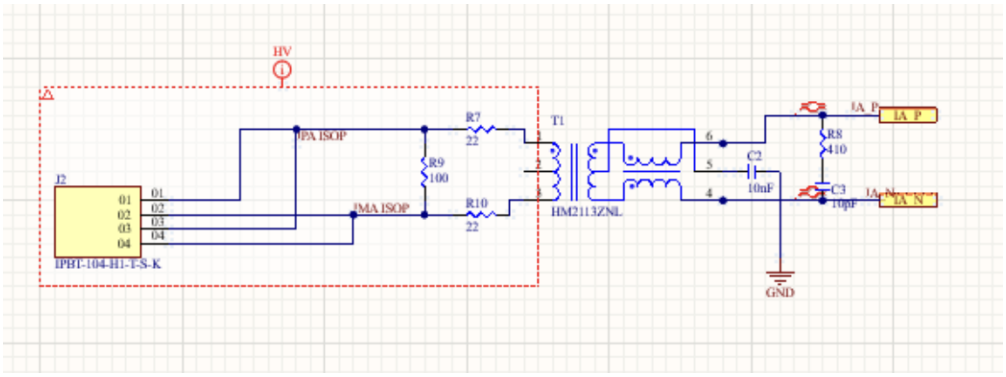

Figure 10: isoSPI Communication Circuit

B.2 PCB Design for the Slave Board

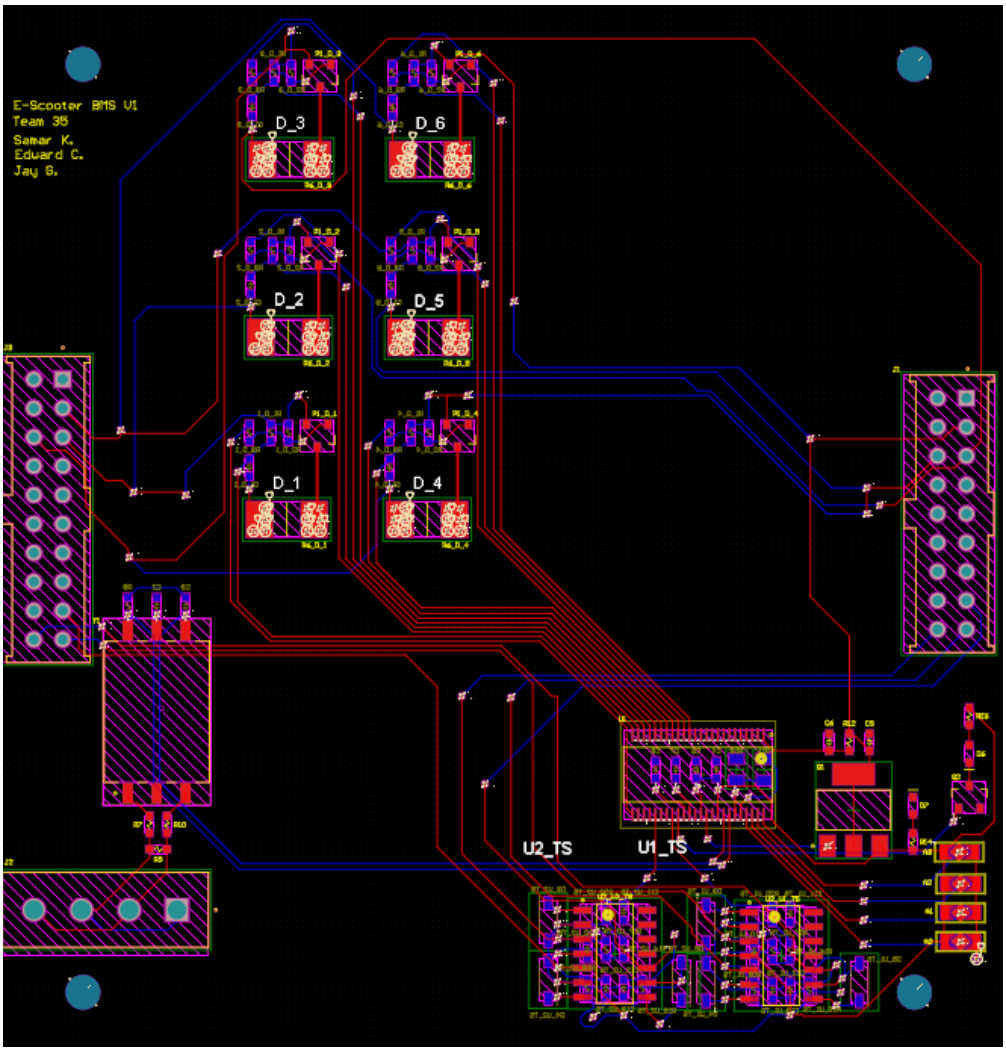

Figure 11: Slave Board PCB Design

B.3 Design Verification for the Slave Board

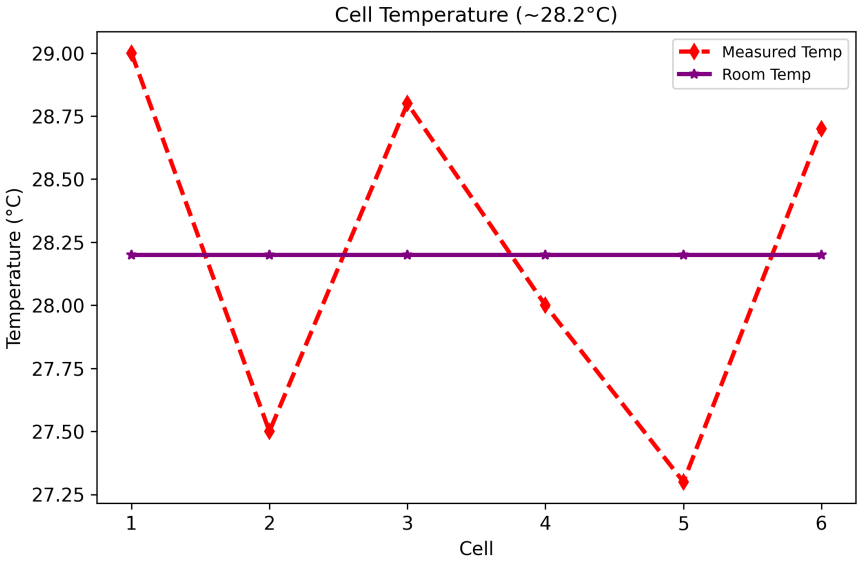

Figure 12: Temperature Sensing Verification

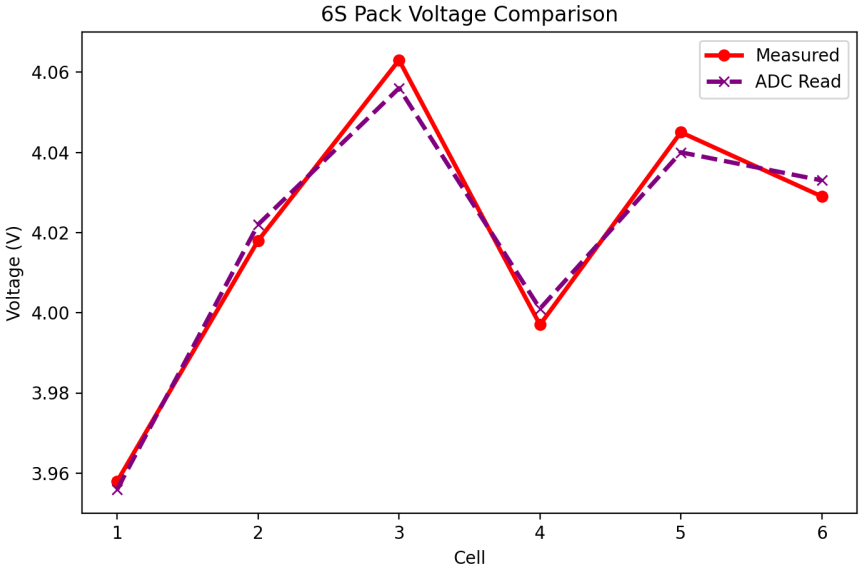

Figure 13: Voltage Sensing Verification

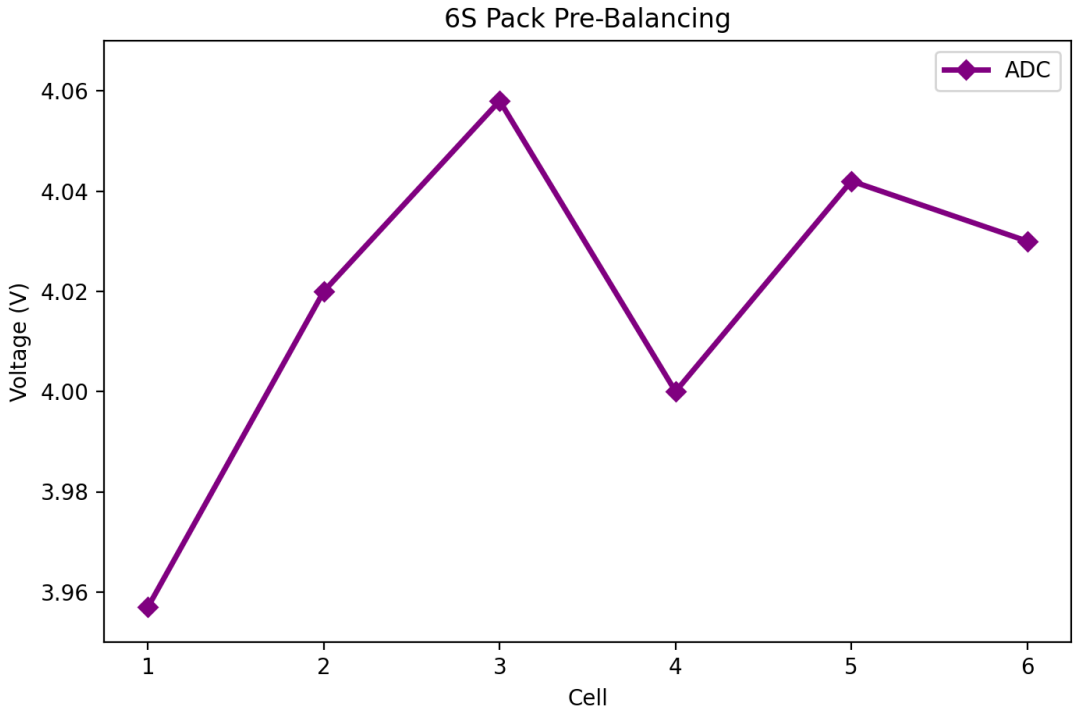

Figure 14: Passive Balancing Verification: Pre-Balancing

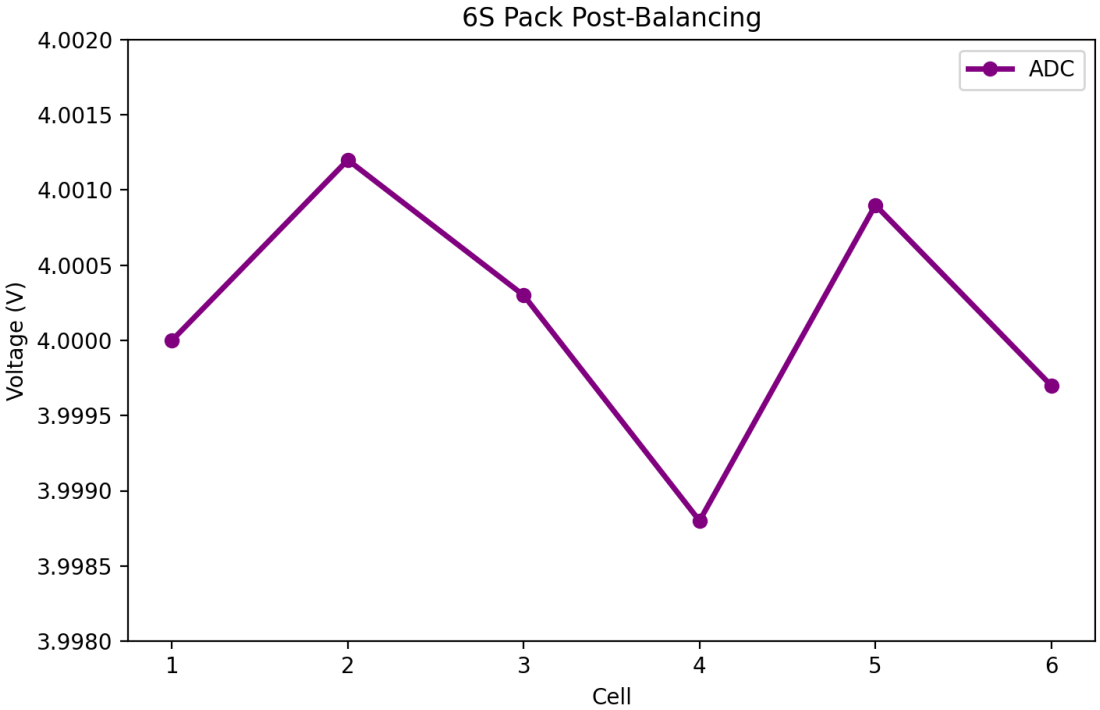

Figure 15: Passive Balancing Verification: Post-Balancing

Appendix C Master Board Subsystem

C.1 PCB Schematic for the Master Board

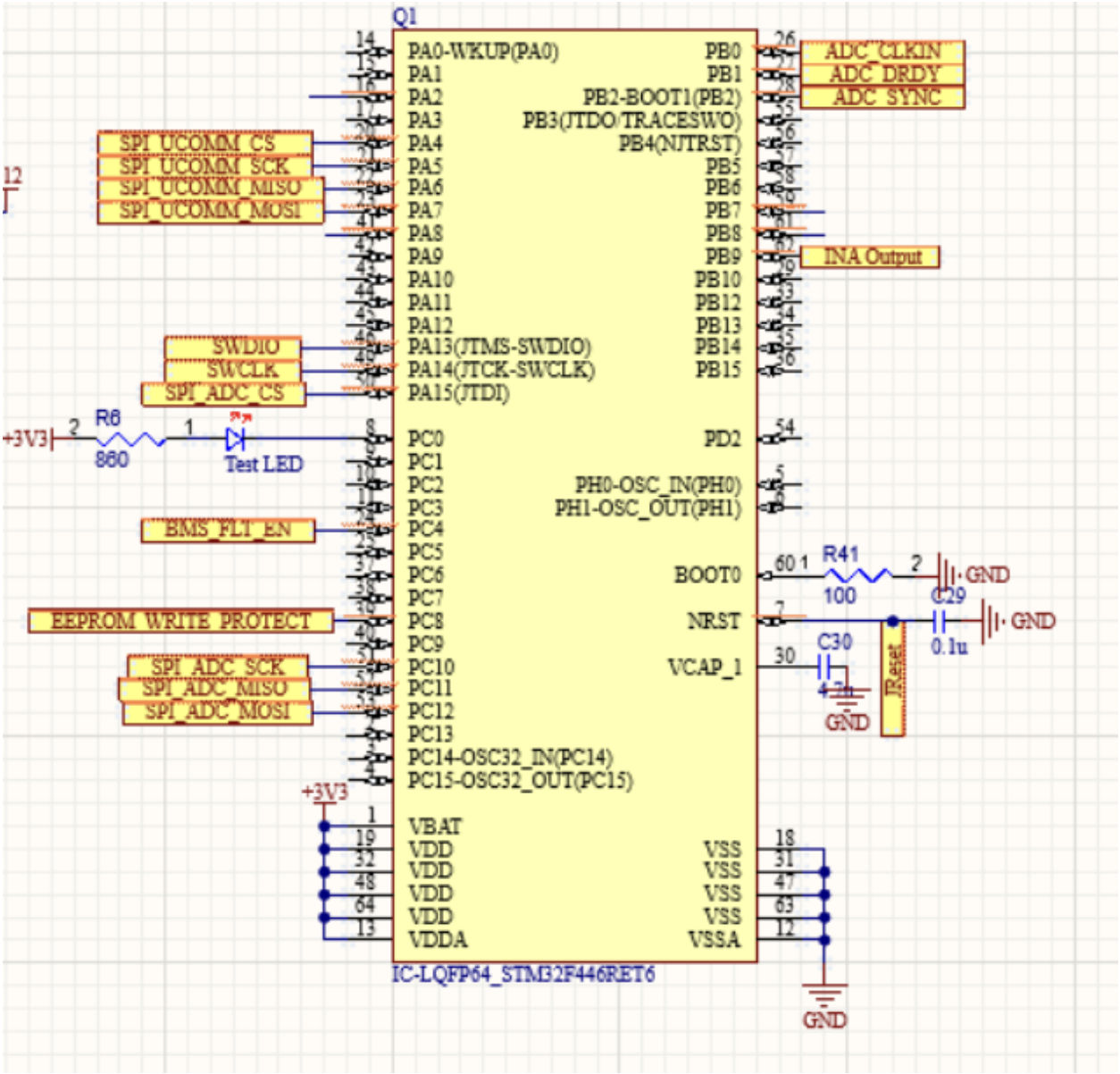

Figure 16: STM32F446 MCU Circuit

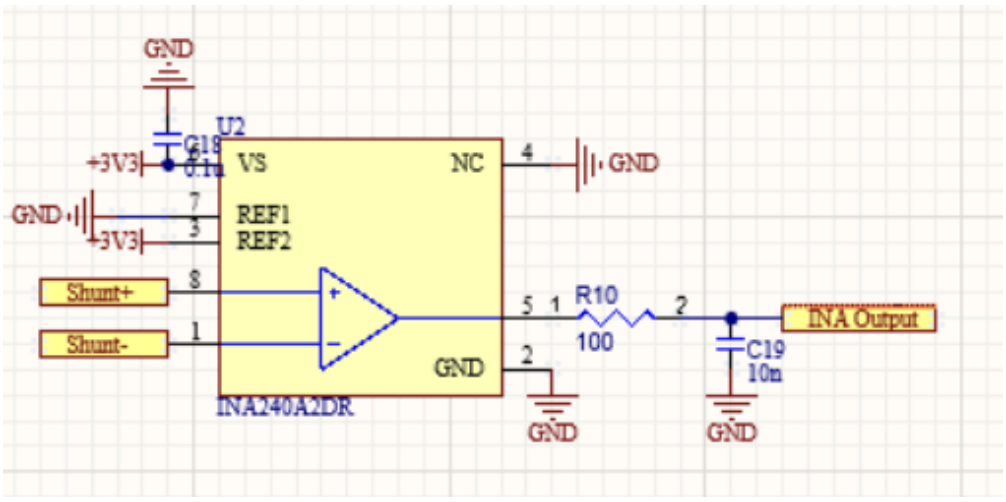

Figure 17: Current Sensing Circuit

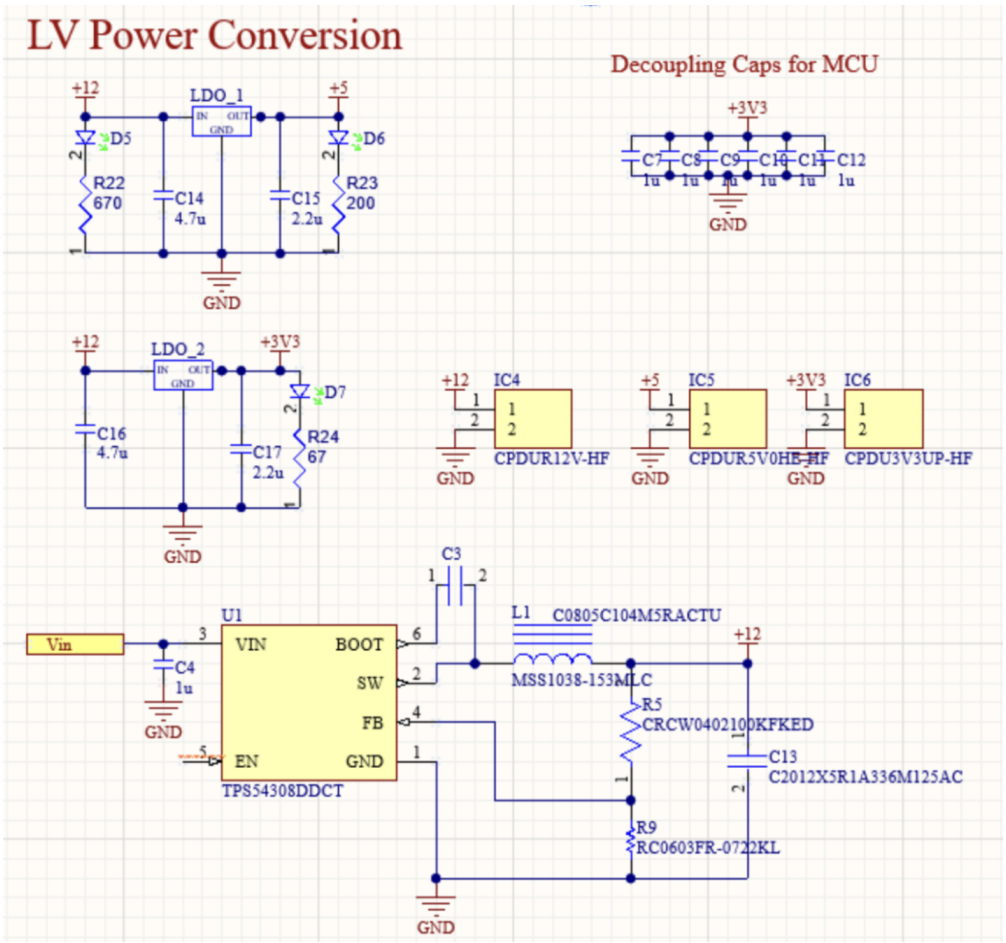

Figure 18: Power Tree Circuit

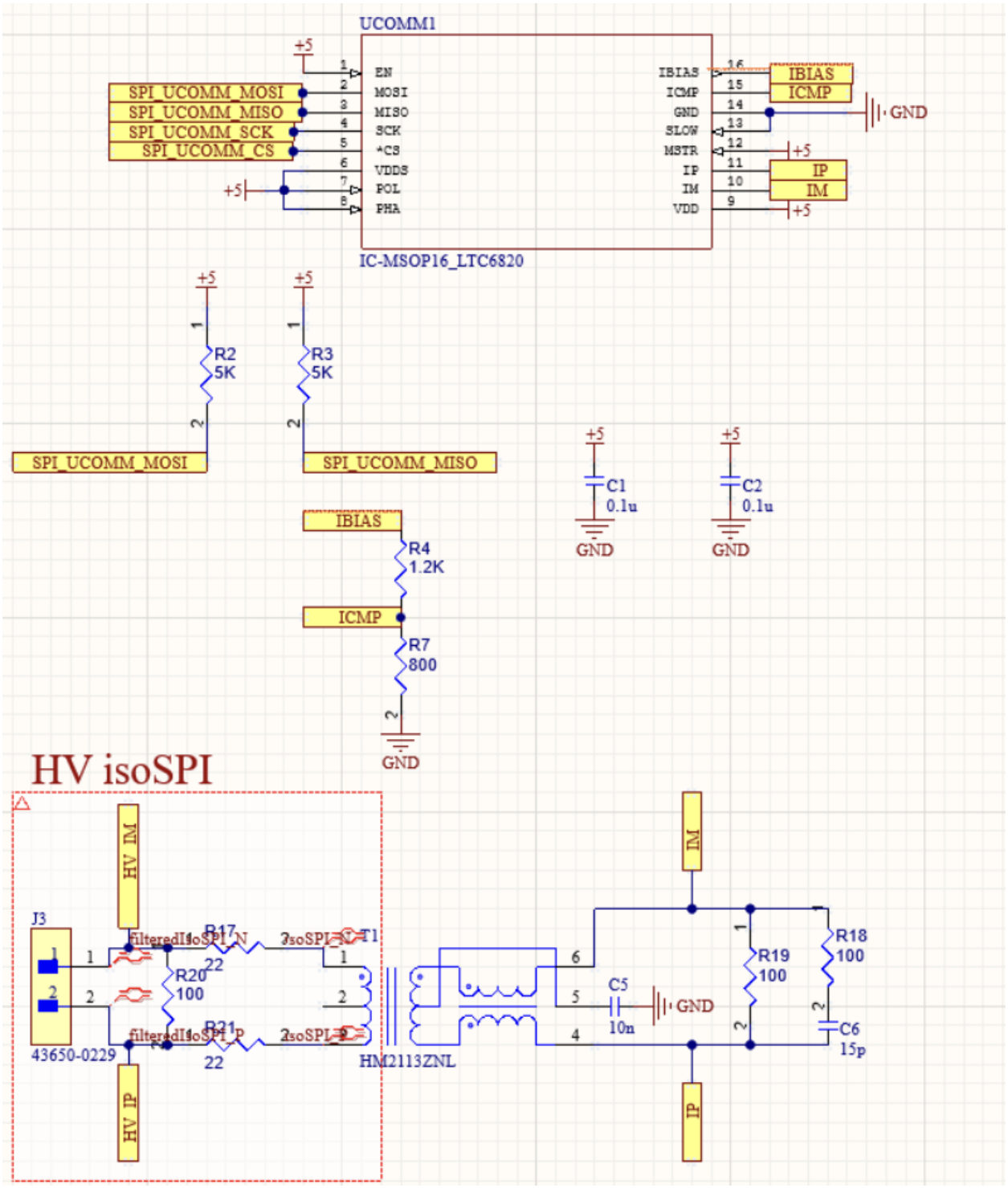

Figure 19: isoSPI Communication Circuit

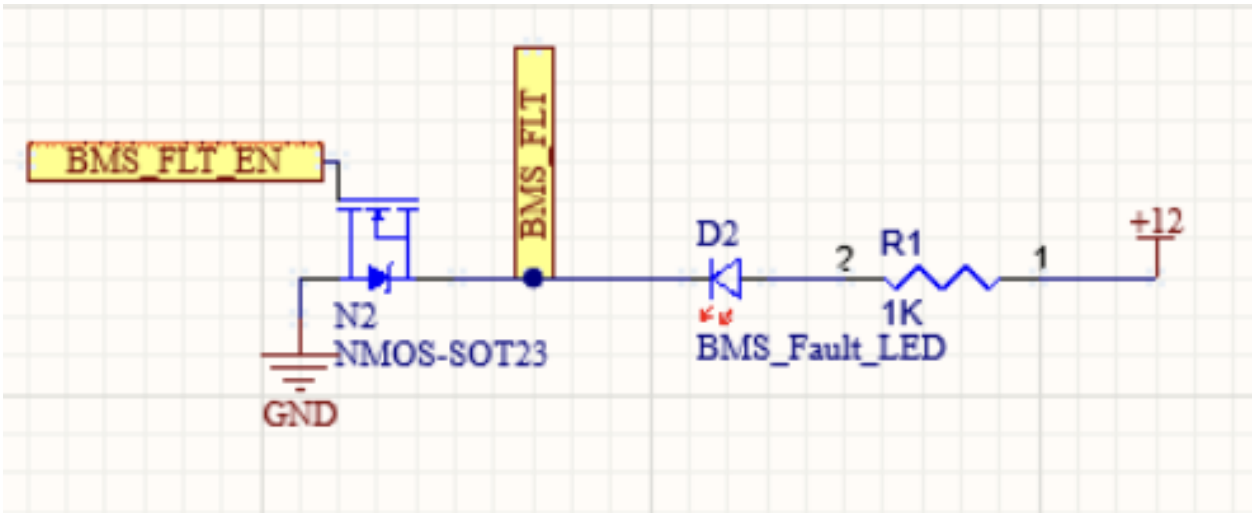

Figure 20: Fault Signal Circuit

C.2 PCB Design for the Master Board

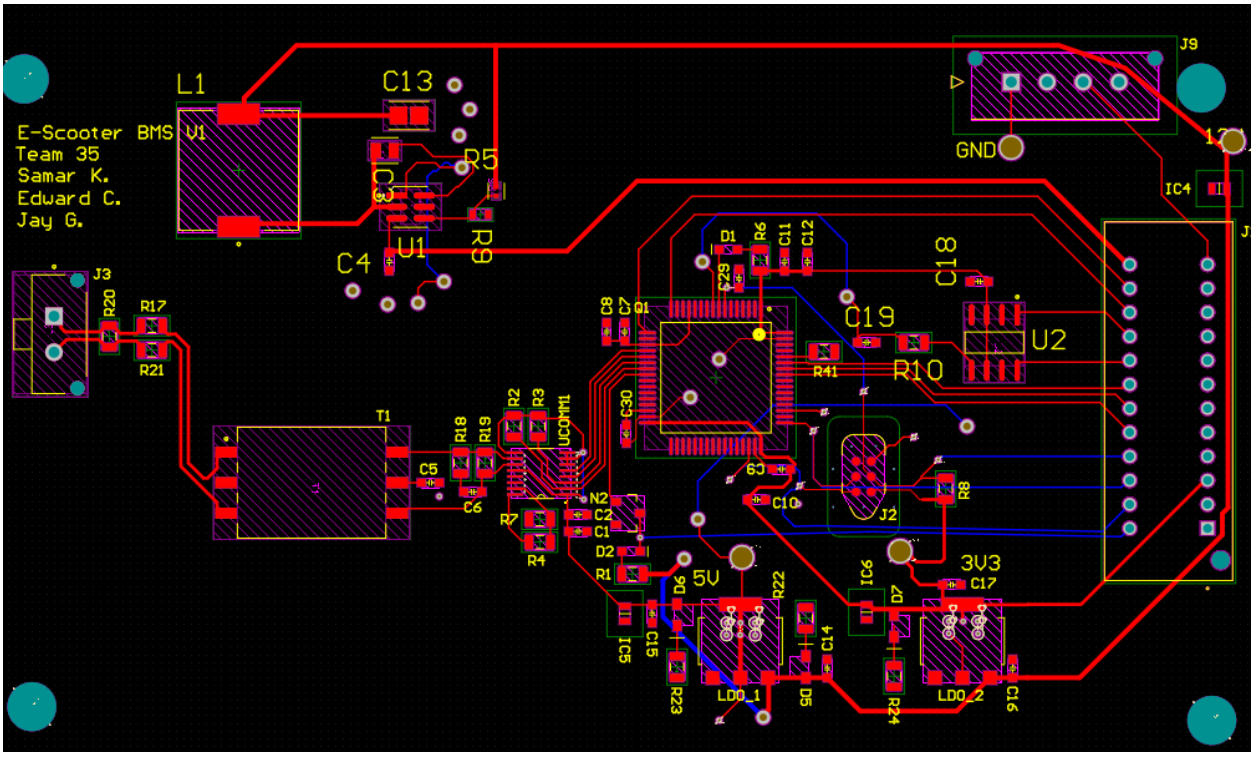

Figure 21: Master Board PCB Design

C.3 Design Verification for the Master Board

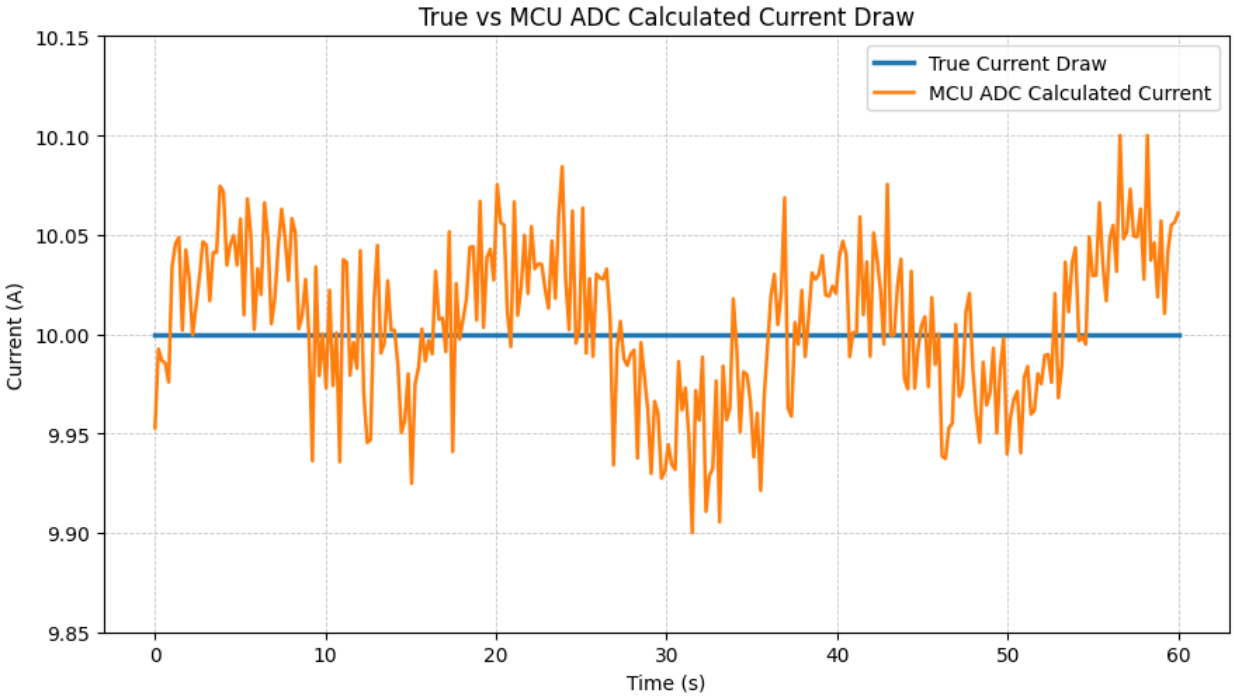

Figure 22: Current Sensing Verification

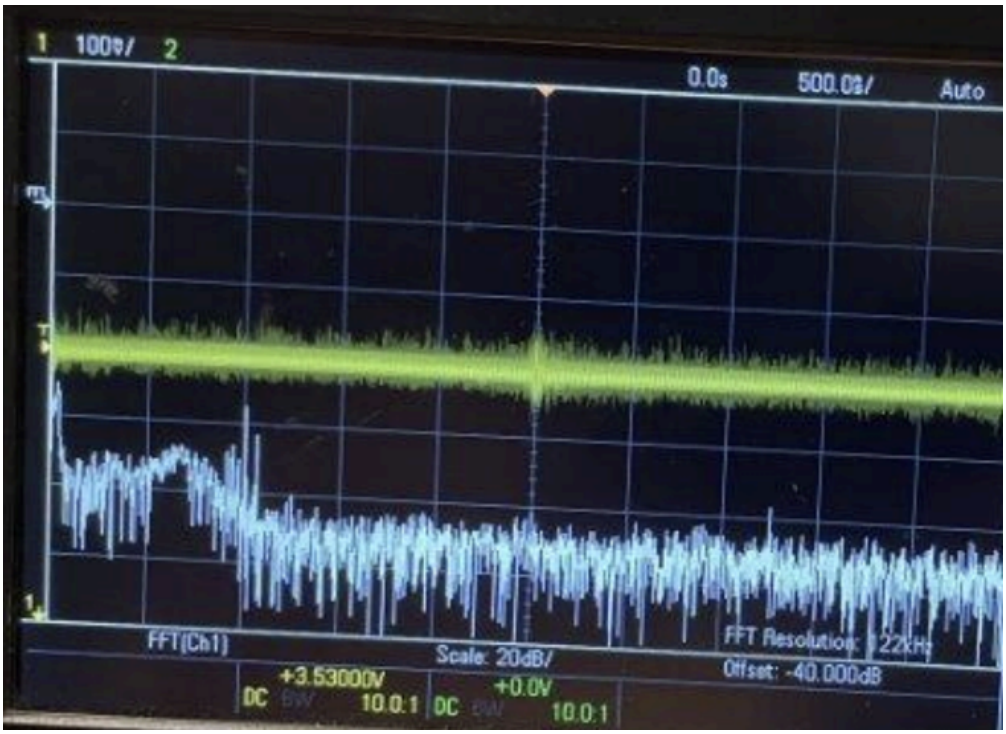

Figure 23: 5V Rail Verification

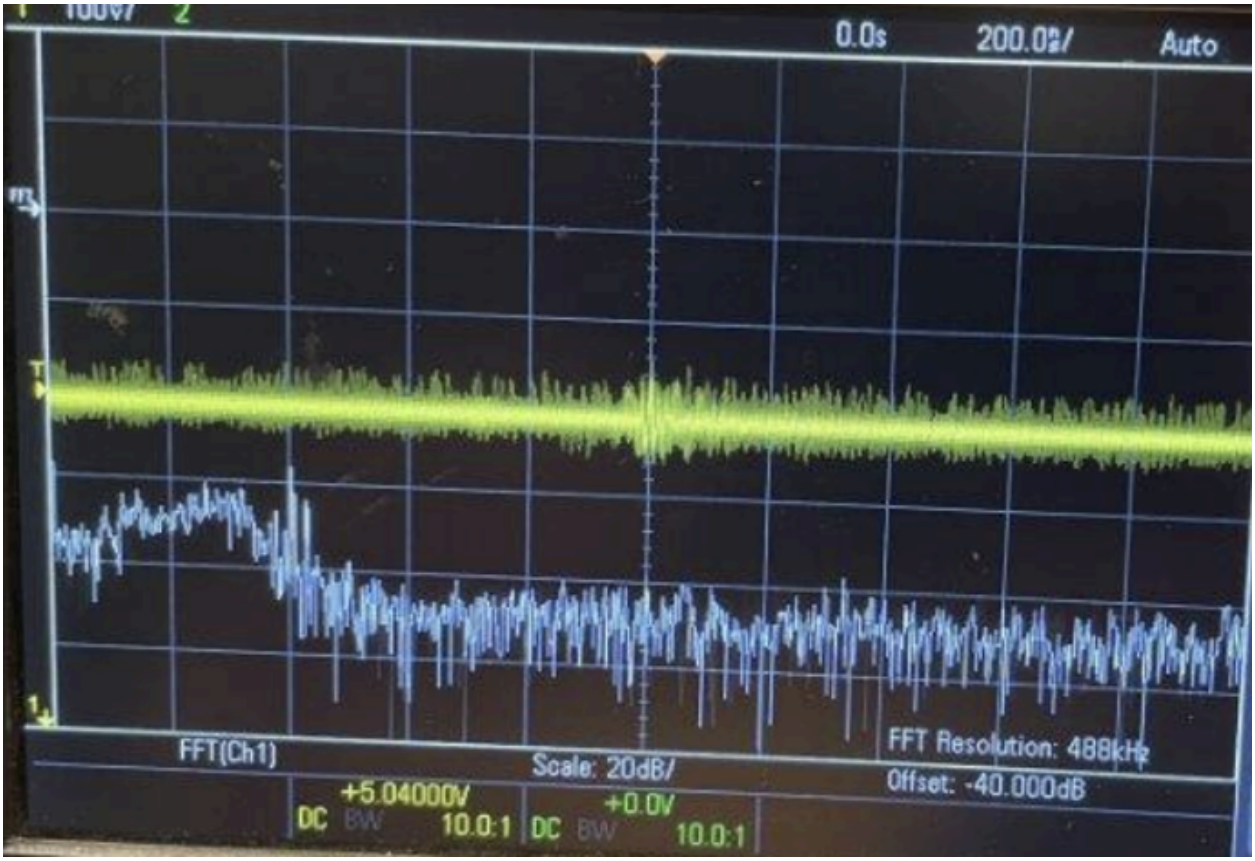

Figure 24: 3.3V Rail Verification

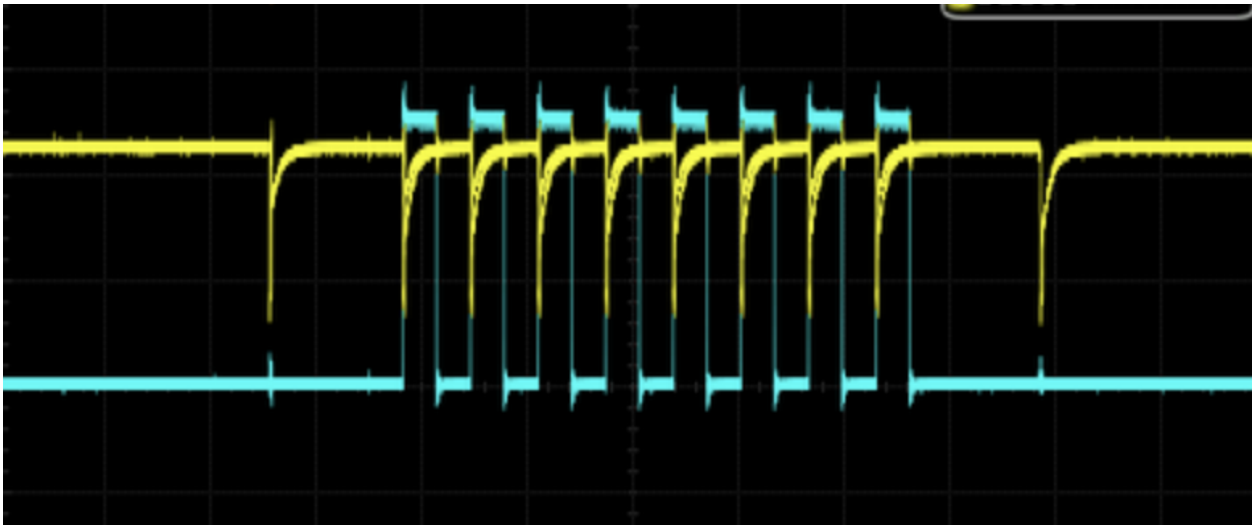
Figure 25: isoSPI Verification

Appendix D BMS Viewer Subsystem

D.1 Live BMS Viewer Dashboard UI

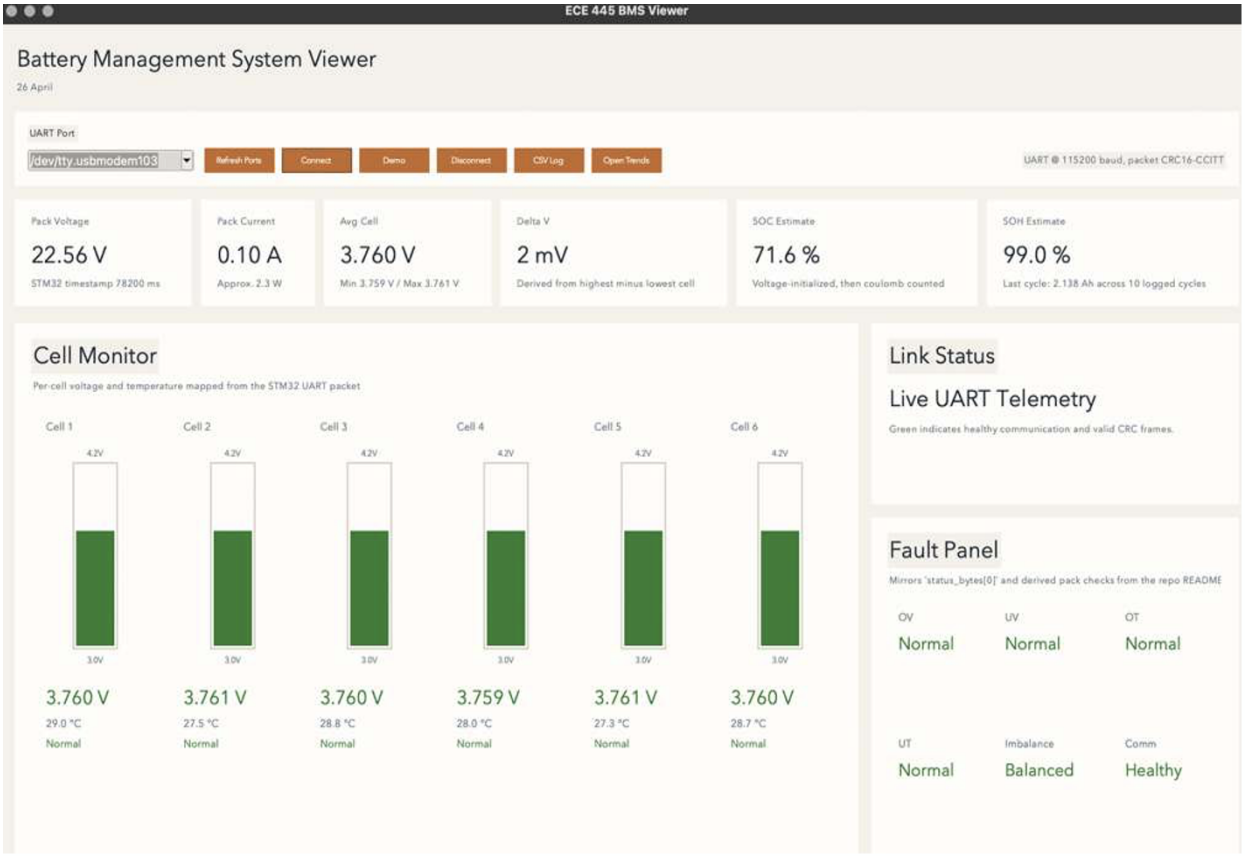

Figure 26: Live BMS Viewer Dashboard UI