

## ECE-483

### Instructions for running demo files

To run the simulations first download both the files in your ece483.work folder and there you will find a "cds.lib".

Open the cds.lib file using vi editor (vi cds.lib) or gedit (gedit cds.lib) using the command that I gave in the bracket or using the GUI.

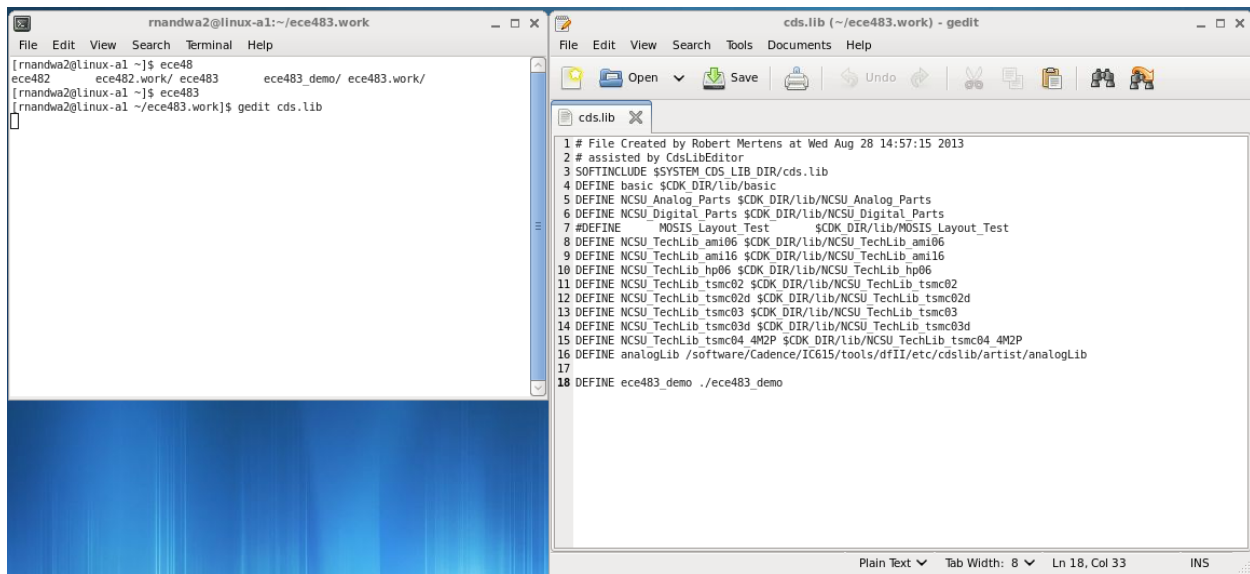
Add the following line at the end of the cds.lib file

```
DEFINE ece483_demo ./ece483_demo
```

(Don't forget the "." before "/")

Then when you will run virtuoso you can see ece483\_demo library in the library manager.

I have also uploaded a screen shot for how the cds.lib file will look after you add then new library.



```
File Created by Robert Mertens at Wed Aug 28 14:57:15 2013
# assisted by CdsLibEditor
SOFTINCLUDE $SYSTEM_CDS_LIB_DIR/cds.lib
DEFINE basic $CDK_DIR/lib/basic
DEFINE NCSU_Analog_Parts $CDK_DIR/lib/NCSU_Analog_Parts
DEFINE NCSU_Digital_Parts $CDK_DIR/lib/NCSU_Digital_Parts
#DEFINE M0SIS_Layout_Test $CDK_DIR/lib/M0SIS_Layout_Test
DEFINE NCSU_TechLib_ami06 $CDK_DIR/lib/NCSU_TechLib_ami06
DEFINE NCSU_TechLib_ami16 $CDK_DIR/lib/NCSU_TechLib_ami16
DEFINE NCSU_TechLib_hp06 $CDK_DIR/lib/NCSU_TechLib_hp06
DEFINE NCSU_TechLib_tsmc02 $CDK_DIR/lib/NCSU_TechLib_tsmc02
DEFINE NCSU_TechLib_tsmc02d $CDK_DIR/lib/NCSU_TechLib_tsmc02d
DEFINE NCSU_TechLib_tsmc03 $CDK_DIR/lib/NCSU_TechLib_tsmc03
DEFINE NCSU_TechLib_tsmc03d $CDK_DIR/lib/NCSU_TechLib_tsmc03d
DEFINE NCSU_TechLib_tsmc04_4M2P $CDK_DIR/lib/NCSU_TechLib_tsmc04_4M2P
DEFINE analogLib /software/Cadence/TC615/tools/dfII/etc/cdslib/artist/analogLib
17
18 DEFINE ece483_demo ./ece483_demo
```

Now you can see the Layout and extracted simulation schematic and saved states for running different simulations.

For HW#5 Q-1 you can see that there are three test benches.

- 1) With DC sweep in dc simulation options
- 2) DC sweep with parametric simulation
- 3) With feedback loop

If you open any schematic file you will find that for all the schematics I have written some notes on the schematic itself about how to run the simulations.

But just in case if you dont remember the general way is go to Launch-> ADE-L-> Session- -> load state and then load the state from the cellview.

## Helpful links for simulation tutorials

For your reference I am also providing the link of the two webpages that might help you in layout and simulation.

<http://web.engr.oregonstate.edu/~moon/ece423/cadence/>

This first link from Oregon State University has an example of designing a common source amplifier with 0.25µm process. You can follow this example for learning about the layout.

Few things to remember while using this example

- 1) They use 0.25µm process so the minimum grid size they can use is 62.5nm and its multiples while in our case it's 0.18µm process so the minimum is 45nm and its multiples.
- 2) They use Metal-4 Metal-5 and Via M5\_M4 for capacitor layout. While in our case we should use Metal-5, Metal-6 and Via M6\_M5.
- 3) They run simulations using command line HSPICE while we will do it using ADE and spectre (given in next link)

The second link is from University of Maryland

<http://www.ece.umd.edu/~dilli/research/layout/cadencetutorial/printabletutorial/>

They use a 0.6µm process. However the section-3 (Simulation) and section-6 (extracted simulation) of the tutorial is very useful.